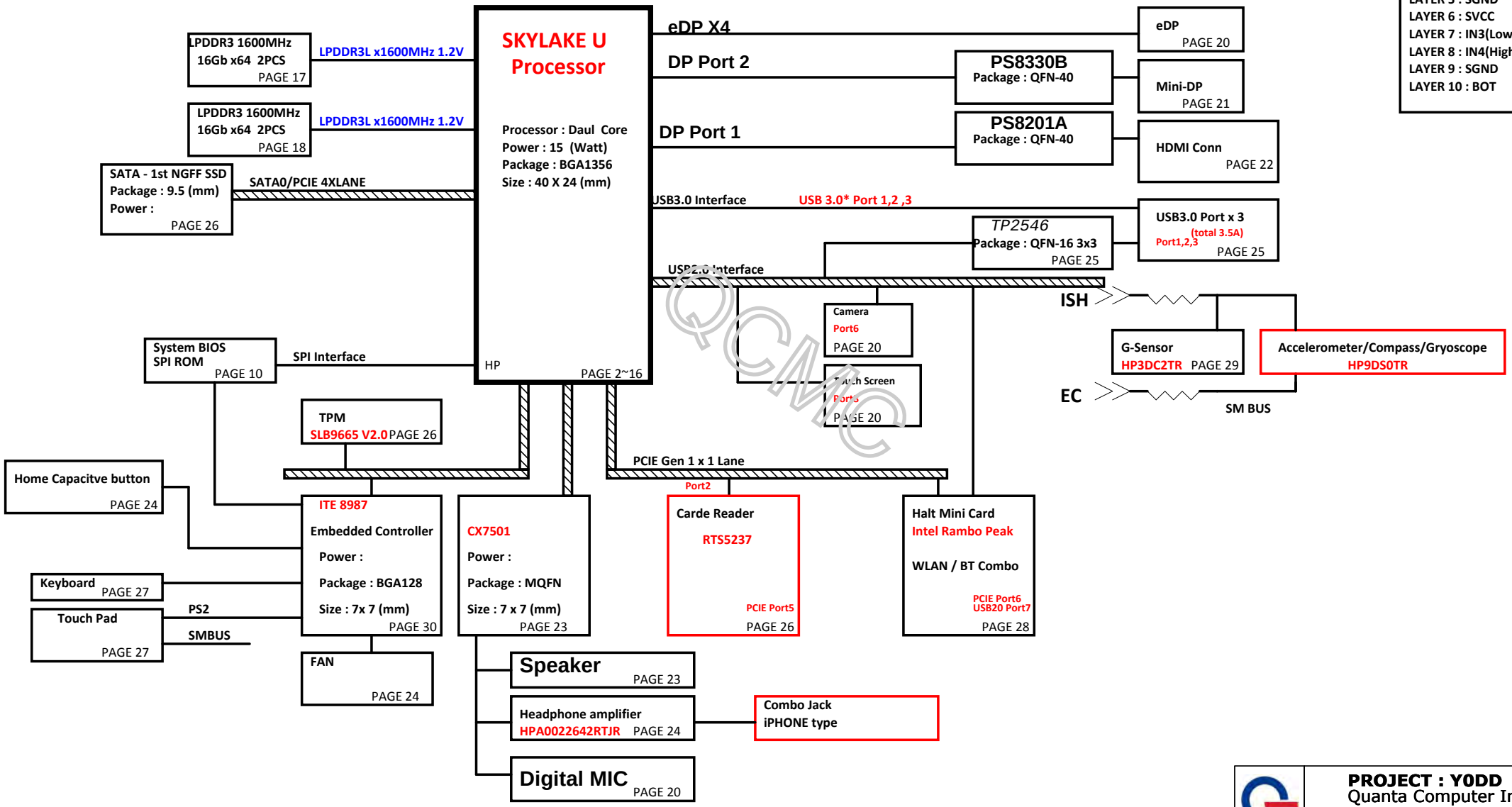
Pike Intel SKYLAKE ULT Platform Block Diagram

PCB 10L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SGND
LAYER 6 : SVCC
LAYER 7 : IN3(Low)
LAYER 8 : IN4(High)
LAYER 9 : SGND
LAYER 10 : BOT



QCMC

NB5

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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HDMI

+3V 4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38
+1.0V 4,6,30,36
+VCCSTPLL 5,6,9,36,38
+VCCIO 6,16,36

INT_DP_SCL R245 2.2K_2
INT_DP_SDA R246 2.2K_2 +3V

DDPB_CTRLDATA/ GPP_E19
Display Port B Detected
This signal has a weak internal pull-down.
0 = Port B is not detected.
1 = Port B is detected.

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.

DDPD_CTRLDATA R51 10K_2

U11A — SKL_ULT ? — Need apply PN

22 IN_D2#	IN_D2#	E55	DDI1_TXN[0]
22 IN_D2	IN_D2	F55	DDI1_TXP[0]
22 IN_D1#	IN_D1#	E58	DDI1_TXN[1]
22 IN_D1	IN_D1	F58	DDI1_TXP[1]
22 IN_D0#	IN_D0#	F53	DDI1_TXN[2]
22 IN_D0	IN_D0	G53	DDI1_TXP[2]
22 IN_CLK#	IN_CLK#	F56	DDI1_TXN[3]
22 IN_CLK	IN_CLK	G56	DDI1_TXP[3]
21 INT_DP_TXN0		C50	DDI2_TXN[0]
21 INT_DP_TXP0		D50	DDI2_TXP[0]
21 INT_DP_TXN1		C52	DDI2_TXN[1]
21 INT_DP_TXP1		D52	DDI2_TXP[1]
21 INT_DP_TXN2		A50	DDI2_TXN[2]
21 INT_DP_TXP2		B50	DDI2_TXP[2]
21 INT_DP_TXN3		D51	DDI2_TXN[3]
21 INT_DP_TXP3		C51	DDI2_TXP[3]
22 SDVO_CLK		L13	GPP_E18/DDPB_CTRLCLK
22 SDVO_DATA		L12	GPP_E19/DDPB_CTRLDATA
21 INT_DP_SCL		N7	GPP_E20/DDPC_CTRLCLK
21 INT_DP_SDA		N8	GPP_E21/DDPC_CTRLDATA
DDPD_CTRLDATA		N11	GPP_E22/DDPD_CTRLCLK
		N12	GPP_E23/DDPD_CTRLDATA
+VCCIO R47 24.9/F_2 EDP_RCOMP		E52	EDP_RCOMP

DDI / DISPLAY SIDEBANDS / EDP

EDP_TXN[0]	C47	INT_EDP_TXN0	INT_EDP_TXN0 20
EDP_TXP[0]	C46	INT_EDP_TXP0	INT_EDP_TXP0 20
EDP_TXN[1]	D46	INT_EDP_TXN1	INT_EDP_TXN1 20
EDP_TXP[1]	C45	INT_EDP_TXP1	INT_EDP_TXP1 20
EDP_TXN[2]	A45	INT_EDP_TXN2	INT_EDP_TXN2 20
EDP_TXP[2]	B45	INT_EDP_TXP2	INT_EDP_TXP2 20
EDP_TXN[3]	A47	INT_EDP_TXN3	INT_EDP_TXN3 20
EDP_TXP[3]	B47	INT_EDP_TXP3	INT_EDP_TXP3 20
EDP_AUXN	E45	INT_EDP_AUXN	INT_EDP_AUXN 20
EDP_AUXP	F45	INT_EDP_AUXP	INT_EDP_AUXP 20
EDP_DISP_UTIL	B52	EDP_DISP_UTIL	TP46
DDI1_AUXN	G50		
DDI1_AUXP	E50		
DDI2_AUXN	E48	INT_DP_AUXN	INT_DP_AUXN 21
DDI2_AUXP	F48	INT_DP_AUXP	INT_DP_AUXP 21
DDI3_AUXN	G46		
DDI3_AUXP	F46		
GPP_E13/DDPB_HPD0	L9	HDMI_HPD_CON	HDMI_HPD_CON 22
GPP_E14/DDPC_HPD1	L7		INT_DP_HPD_Q 21
GPP_E15/DDPD_HPD2	L6		
GPP_E16/DDPE_HPD3	N9		
GPP_E17/EDP_HPD	L10	ULT_EDP_HPD	ULT_EDP_HPD 20
EDP_BKLTEN	R12	PCH_LVDS_BLON	PCH_LVDS_BLON 20
EDP_BKLTCTL	R11	PCH_DPST_PWM	PCH_DPST_PWM 20
EDP_VDDEN	U13	PCH_DISP_ON	PCH_DISP_ON 20

*SKL_ULT
REV = 1
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eDP_COMPIO and iCOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V
R188 *10K_2
ULT_EDP_HPD
R187 100K_2

Mini-DP

+VCCSTPLL
R165 *49.9/F_2 CATERR#
+1.0V
R29 *51_2 JTAGX_PCH
R30 51_2 JTAG_TMS_PCH
R35 51_2 JTAG_TDI_PCH
R25 51_2 JTAG_TDO_PCH
R23 51_2 JTAG_TCK_PCH
Close to Chipset

30,32,38 H_PROCHOT# R164 499/F_4
30 EC_PECI
30 PM_THRMTRIP#

TP1134 XDP_BPM0 C55
TP1135 XDP_BPM1 D55
B54
C56

TP45 CPU_GP0 A6
TP47 CPU_GP1 A7
TP35 CPU_GP2 BA5
TP34 CPU_GP3 AY5

R61 49.9/F_2 PROC_POPIRCOMP AT16
R58 49.9/F_2 PCH_OPI_RCOMP AU16
R48 49.9/F_2 EDRAM_OPIO_RCOMP H66
R45 49.9/F_2 EOPIO_RCOMP H65

U11D — SKL_ULT ? — Need apply PN

CATERR#	D61	
EC_PECI	A64	
PROCHOT#	C63	
PM_THRMTRIP#	A63	
SKTOCC#	A65	
GPP_E3/CPU_GP0	A6	
GPP_E7/CPU_GP1	A7	
GPP_B3/CPU_GP2	BA5	
GPP_B4/CPU_GP3	AY5	
PROC_POPIRCOMP	AT16	
PCH_OPIRCOMP	AU16	
OPCE_RCOMP	H66	
OPC_RCOMP	H65	
PROC_TCK	B61	XDP_TCK0
PROC_TDI	D60	XDP_TDI_CPU
PROC_TDO	A61	XDP_TDO_CPU
PROC_TMS	C60	XDP_TMS_CPU
PROC_TRST#	B59	XDP_TRST#_CPU → XDP_TRST#_CPU 2
PCH_JTAG_TCK	B56	JTAG_TCK_PCH
PCH_JTAG_TDI	D59	JTAG_TDI_PCH
PCH_JTAG_TDO	A56	JTAG_TDO_PCH
PCH_JTAG_TMS	C59	JTAG_TMS_PCH
PCH_TRST#	C61	XDP_TRST#_CPU → XDP_TRST#_CPU 2
JTAGX	A59	JTAGX_PCH

*SKL_ULT
REV = 1
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Close to EC
+VCCSTPLL
PM_THRMTRIP# R213 1K_4
Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU
+1.0V
XDP_TMS_CPU R36 *51_2
XDP_TDI_CPU R31 *51_2
XDP_TDO_CPU R28 *51_2

+1.0V
H_PROCHOT# R142 1K_2
XDP_TCK0 R177 51_2
XDP_TRST#_CPU R27 51_2

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NB5

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SKLU (1/14)	1A

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SkyLake ULT Processor (DDR3L)

17 M_A_DQSN[7:0]
17 M_A_DQSP[7:0]
18 M_B_DQSN[7:0]
18 M_B_DQSP[7:0]
17 M_A_DQ[63:0]
18 M_B_DQ[63:0]

+1.2VSUS 6,17,18,34,36

Need apply PN

U11B — SKL_ULT — 2 OF 20

M_A_DQ0	AL71	DDR0_DQ[0]	DDR0_CKN[0]	AU53	M_A_CLKN0 17,19
M_A_DQ1	AL68	DDR0_DQ[1]	DDR0_CKP[0]	AT53	M_A_CLKP0 17,19
M_A_DQ2	AN68	DDR0_DQ[2]	DDR0_CKN[1]	AU55	M_A_CLKN1 17,19
M_A_DQ3	AN69	DDR0_DQ[3]	DDR0_CKP[1]	AT55	M_A_CLKP1 17,19
M_A_DQ4	AL70	DDR0_DQ[4]		BA56	
M_A_DQ5	AL69	DDR0_DQ[5]	DDR0_CKE[0]	BB56	M_A_CKE0 17,19
M_A_DQ6	AN70	DDR0_DQ[6]	DDR0_CKE[1]	AW56 M_A_CKE2	M_A_CKE1 17,19
M_A_DQ7	AN71	DDR0_DQ[7]	DDR0_CKE[2]	AY56 M_A_CKE3	M_A_CKE2 17,19
M_A_DQ8	AR70	DDR0_DQ[8]	DDR0_CKE[3]		M_A_CKE3 17,19
M_A_DQ9	AR68	DDR0_DQ[9]		AU45	
M_A_DQ10	AU71	DDR0_DQ[10]	DDR0_CS#[0]	AU43	M_A_CS#0 17,19
M_A_DQ11	AU68	DDR0_DQ[11]	DDR0_CS#[1]	AT45	M_A_CS#1 17,19
M_A_DQ12	AR71	DDR0_DQ[12]	DDR0_ODT[0]	AT43	M_A_ODT0 17,19
M_A_DQ13	AR69	DDR0_DQ[13]	DDR0_ODT[1]		
M_A_DQ14	AU70	DDR0_DQ[14]		BA51 M_A_A0	M_A_A0 17,19
M_A_DQ15	AU69	DDR0_DQ[15]	DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	BB54 M_A_A1	M_A_A1 17,19
M_A_DQ16	AF65	DDR1_DQ[0]/DDR0_DQ[16]	DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	BA52 M_A_A2	M_A_A2 17,19
M_A_DQ17	AF64	DDR1_DQ[1]/DDR0_DQ[17]	DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]	AY52 M_A_A3	M_A_A3 17,19
M_A_DQ18	AK65	DDR1_DQ[2]/DDR0_DQ[18]	DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]	AW52 M_A_A4	M_A_A4 17,19
M_A_DQ19	AK64	DDR1_DQ[3]/DDR0_DQ[19]	DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	AV55 M_A_A5	M_A_A5 17,19
M_A_DQ20	AF66	DDR1_DQ[4]/DDR0_DQ[20]	DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]	AW54 M_A_A6	M_A_A6 17,19
M_A_DQ21	AF67	DDR1_DQ[5]/DDR0_DQ[21]	DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	BA54 M_A_A7	M_A_A7 17,19
M_A_DQ22	AK67	DDR1_DQ[6]/DDR0_DQ[22]	DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]	BA55 M_A_A8	M_A_A8 17,19
M_A_DQ23	AK66	DDR1_DQ[7]/DDR0_DQ[23]	DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#	AY54 M_A_A9	M_A_A9 17,19
M_A_DQ24	AF70	DDR1_DQ[8]/DDR0_DQ[24]	DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]		
M_A_DQ25	AF68	DDR1_DQ[9]/DDR0_DQ[25]		AU46 M_A_B0	M_A_B0 17,19
M_A_DQ26	AH71	DDR1_DQ[10]/DDR0_DQ[26]	DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]	AU48 M_A_B1	M_A_B1 17,19
M_A_DQ27	AH68	DDR1_DQ[11]/DDR0_DQ[27]	DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	AT46 M_A_B2	M_A_B2 17,19
M_A_DQ28	AH71	DDR1_DQ[12]/DDR0_DQ[28]	DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	AU50 M_A_B3	M_A_B3 17,19
M_A_DQ29	AH69	DDR1_DQ[13]/DDR0_DQ[29]	DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	AU52 M_A_B4	M_A_B4 17,19
M_A_DQ30	AH70	DDR1_DQ[14]/DDR0_DQ[30]	DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	AY51 M_A_B5	M_A_B5 17,19
M_A_DQ31	AH69	DDR1_DQ[15]/DDR0_DQ[31]	DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	AT48 M_A_B6	M_A_B6 17,19
M_A_DQ32	BB65	DDR1_DQ[16]/DDR0_DQ[32]	DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]	AT50 M_A_B7	M_A_B7 17,19
M_A_DQ33	AW65	DDR1_DQ[17]/DDR0_DQ[33]	DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]	BB50 M_A_B8	M_A_B8 17,19
M_A_DQ34	AW63	DDR1_DQ[18]/DDR0_DQ[34]	DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	AY50 M_A_B9	M_A_B9 17,19
M_A_DQ35	AY63	DDR1_DQ[19]/DDR0_DQ[35]	DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	BA50	
M_A_DQ36	BA65	DDR1_DQ[20]/DDR0_DQ[36]	DDR0_MA[3]	BB52	
M_A_DQ37	AY65	DDR1_DQ[21]/DDR0_DQ[37]	DDR0_MA[4]		
M_A_DQ38	BA63	DDR1_DQ[22]/DDR0_DQ[38]		AM70 M_A_DQSN0	
M_A_DQ39	BB63	DDR1_DQ[23]/DDR0_DQ[39]	DDR0_DQSP[0]	AM69 M_A_DQSP0	
M_A_DQ40	BA61	DDR1_DQ[24]/DDR0_DQ[40]	DDR0_DQSN[1]	AT69 M_A_DQSN1	
M_A_DQ41	AW61	DDR1_DQ[25]/DDR0_DQ[41]	DDR0_DQSP[1]	AT70 M_A_DQSP1	
M_A_DQ42	BB59	DDR1_DQ[26]/DDR0_DQ[42]	DDR1_DQSN[0]/DDR0_DQSN[2]	AH66 M_A_DQSN2	
M_A_DQ43	AW59	DDR1_DQ[27]/DDR0_DQ[43]	DDR1_DQSP[0]/DDR0_DQSP[2]	AH65 M_A_DQSP2	
M_A_DQ44	BB61	DDR1_DQ[28]/DDR0_DQ[44]	DDR1_DQSN[1]/DDR0_DQSN[3]	AG69 M_A_DQSN3	
M_A_DQ45	AY61	DDR1_DQ[29]/DDR0_DQ[45]	DDR1_DQSP[1]/DDR0_DQSP[3]	AG70 M_A_DQSP3	
M_A_DQ46	BA59	DDR1_DQ[30]/DDR0_DQ[46]	DDR0_DQSN[2]/DDR0_DQSN[4]	BA64 M_A_DQSN4	
M_A_DQ47	AY59	DDR1_DQ[31]/DDR0_DQ[47]	DDR0_DQSP[2]/DDR0_DQSP[4]	AY64 M_A_DQSP4	
M_A_DQ48	AT66	DDR1_DQ[16]/DDR0_DQ[48]	DDR0_DQSN[3]/DDR0_DQSN[5]	AV60 M_A_DQSN5	
M_A_DQ49	AU66	DDR1_DQ[17]/DDR0_DQ[49]	DDR0_DQSP[3]/DDR0_DQSP[5]	BA60 M_A_DQSP5	
M_A_DQ50	AP65	DDR1_DQ[18]/DDR0_DQ[50]	DDR1_DQSN[2]/DDR0_DQSN[6]	AR66 M_A_DQSN6	
M_A_DQ51	AN65	DDR1_DQ[19]/DDR0_DQ[51]	DDR1_DQSP[2]/DDR0_DQSP[6]	AR65 M_A_DQSP6	
M_A_DQ52	AN66	DDR1_DQ[20]/DDR0_DQ[52]	DDR1_DQSN[3]/DDR0_DQSN[7]	AR61 M_A_DQSN7	
M_A_DQ53	AP66	DDR1_DQ[21]/DDR0_DQ[53]	DDR1_DQSP[3]/DDR0_DQSP[7]	AR60 M_A_DQSP7	
M_A_DQ54	AT65	DDR1_DQ[22]/DDR0_DQ[54]			
M_A_DQ55	AU65	DDR1_DQ[23]/DDR0_DQ[55]			
M_A_DQ56	AT61	DDR1_DQ[24]/DDR0_DQ[56]			
M_A_DQ57	AU61	DDR1_DQ[25]/DDR0_DQ[57]			
M_A_DQ58	AP60	DDR1_DQ[26]/DDR0_DQ[58]			
M_A_DQ59	AN60	DDR1_DQ[27]/DDR0_DQ[59]			
M_A_DQ60	AN61	DDR1_DQ[28]/DDR0_DQ[60]			
M_A_DQ61	AP61	DDR1_DQ[29]/DDR0_DQ[61]			
M_A_DQ62	AT60	DDR1_DQ[30]/DDR0_DQ[62]			
M_A_DQ63	AU60	DDR1_DQ[31]/DDR0_DQ[63]			

NIL-DDR CH - A

DDR0_ALERT# AW50
DDR0_PAR AT52

DDR_VREF_CA AY67 — SM_VREF_CA 17
DDR0_VREF_DQ AY68 — SM_VREF_DQ0 17
DDR1_VREF_DQ BA67 — SM_VREF_DQ1 18

20mils width

DDR_VTT_CNTL AW67 — DDR_VTT_CNTL R597 *0_2 — DDR_VTT_CNTL_R 4

Place near CPU

*SKL_ULT
REV = 1

U11C — SKL_ULT — 3 OF 20

Need apply PN

M_B_DQ0	AY39	DDR0_DQ[32]/DDR1_DQ[0]	DDR1_CKN[0]	AN45	M_B_CLKN0 18,19
M_B_DQ1	AW39	DDR0_DQ[33]/DDR1_DQ[1]	DDR1_CKN[1]	AN46	M_B_CLKN1 18,19
M_B_DQ2	AY37	DDR0_DQ[34]/DDR1_DQ[2]	DDR1_CKP[0]	AP45	M_B_CLKP0 18,19
M_B_DQ3	AW37	DDR0_DQ[35]/DDR1_DQ[3]	DDR1_CKP[1]	AP46	M_B_CLKP1 18,19
M_B_DQ4	BB39	DDR0_DQ[36]/DDR1_DQ[4]		AN56	
M_B_DQ5	BA39	DDR0_DQ[37]/DDR1_DQ[5]	DDR1_CKE[0]	AP55	M_B_CKE0 18,19
M_B_DQ6	BA37	DDR0_DQ[38]/DDR1_DQ[6]	DDR1_CKE[1]	AN55 M_B_CKE2	M_B_CKE1 18,19
M_B_DQ7	BB37	DDR0_DQ[39]/DDR1_DQ[7]	DDR1_CKE[2]	AP53 M_B_CKE3	M_B_CKE2 18,19
M_B_DQ8	AY35	DDR0_DQ[40]/DDR1_DQ[8]	DDR1_CKE[3]		M_B_CKE3 18,19
M_B_DQ9	AW35	DDR0_DQ[41]/DDR1_DQ[9]		BB42	
M_B_DQ10	AY33	DDR0_DQ[42]/DDR1_DQ[10]	DDR1_CS#[0]	AY42	M_B_CS#0 18,19
M_B_DQ11	AW33	DDR0_DQ[43]/DDR1_DQ[11]	DDR1_CS#[1]	BA42	M_B_CS#1 18,19
M_B_DQ12	BB35	DDR0_DQ[44]/DDR1_DQ[12]	DDR1_ODT[0]	BA43	M_B_ODT0 18,19
M_B_DQ13	BA35	DDR0_DQ[45]/DDR1_DQ[13]	DDR1_ODT[1]	AW42	
M_B_DQ14	BA33	DDR0_DQ[46]/DDR1_DQ[14]		AY48 M_B_A0	
M_B_DQ15	BB33	DDR0_DQ[47]/DDR1_DQ[15]	DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]	AP50 M_B_A1	M_B_A0 18,19
M_B_DQ16	AU40	DDR1_DQ[32]/DDR1_DQ[16]	DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]	BA48 M_B_A2	M_B_A1 18,19
M_B_DQ17	AT40	DDR1_DQ[33]/DDR1_DQ[17]	DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]	BB48 M_B_A3	M_B_A2 18,19
M_B_DQ18	AT37	DDR1_DQ[34]/DDR1_DQ[18]	DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]	AP48 M_B_A4	M_B_A3 18,19
M_B_DQ19	AU37	DDR1_DQ[35]/DDR1_DQ[19]	DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]	AP52 M_B_A5	M_B_A4 18,19
M_B_DQ20	AR40	DDR1_DQ[36]/DDR1_DQ[20]	DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]	AN50 M_B_A6	M_B_A5 18,19
M_B_DQ21	AP40	DDR1_DQ[37]/DDR1_DQ[21]	DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]	AN48 M_B_A7	M_B_A6 18,19
M_B_DQ22	AP37	DDR1_DQ[38]/DDR1_DQ[22]	DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]	AN53 M_B_A8	M_B_A7 18,19
M_B_DQ23	AR37	DDR1_DQ[39]/DDR1_DQ[23]	DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#	AN52 M_B_A9	M_B_A8 18,19
M_B_DQ24	AT33	DDR1_DQ[40]/DDR1_DQ[24]	DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]		M_B_A9 18,19
M_B_DQ25	AU33	DDR1_DQ[41]/DDR1_DQ[25]		BA43 M_B_B0	
M_B_DQ26	AU30	DDR1_DQ[42]/DDR1_DQ[26]	DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]	AY43 M_B_B1	M_B_B0 18,19
M_B_DQ27	AT30	DDR1_DQ[43]/DDR1_DQ[27]	DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	AY44 M_B_B2	M_B_B1 18,19
M_B_DQ28	AR33	DDR1_DQ[44]/DDR1_DQ[28]	DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	AW44 M_B_B3	M_B_B2 18,19
M_B_DQ29	AP33	DDR1_DQ[45]/DDR1_DQ[29]	DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]	BB44 M_B_B4	M_B_B3 18,19
M_B_DQ30	AR30	DDR1_DQ[46]/DDR1_DQ[30]	DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]	AY47 M_B_B5	M_B_B4 18,19
M_B_DQ31	AP30	DDR1_DQ[47]/DDR1_DQ[31]	DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]	BA44 M_B_B6	M_B_B5 18,19
M_B_DQ32	AY31	DDR1_DQ[48]/DDR1_DQ[32]	DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]	AW46 M_B_B7	M_B_B6 18,19
M_B_DQ33	AW31	DDR1_DQ[49]/DDR1_DQ[33]	DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]	AY46 M_B_B8	M_B_B7 18,19
M_B_DQ34	AY29	DDR1_DQ[50]/DDR1_DQ[34]	DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]	BA46 M_B_B9	M_B_B8 18,19
M_B_DQ35	AW29	DDR1_DQ[51]/DDR1_DQ[35]	DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]	BB46	M_B_B9 18,19
M_B_DQ36	BB31	DDR1_DQ[52]/DDR1_DQ[36]	DDR1_MA[3]	BA47	
M_B_DQ37	BA31	DDR1_DQ[53]/DDR1_DQ[37]	DDR1_MA[4]		
M_B_DQ38	BA29	DDR1_DQ[54]/DDR1_DQ[38]		BA38 M_B_DQSN0	
M_B_DQ39	BB29	DDR1_DQ[55]/DDR1_DQ[39]	DDR0_DQSN[4]/DDR1_DQSN[0]	AY38 M_B_DQSP0	
M_B_DQ40	AY27	DDR1_DQ[56]/DDR1_DQ[40]	DDR0_DQSP[4]/DDR1_DQSP[0]	AY34 M_B_DQSN1	
M_B_DQ41	AW27	DDR1_DQ[57]/DDR1_DQ[41]	DDR0_DQSN[5]/DDR1_DQSN[1]	BA34 M_B_DQSP1	
M_B_DQ42	AY25	DDR1_DQ[58]/DDR1_DQ[42]	DDR0_DQSP[5]/DDR1_DQSP[1]	AT38 M_B_DQSN2	
M_B_DQ43	AW25	DDR1_DQ[59]/DDR1_DQ[43]	DDR1_DQSN[4]/DDR1_DQSN[2]	AR38 M_B_DQSP2	
M_B_DQ44	BB27	DDR1_DQ[60]/DDR1_DQ[44]	DDR1_DQSP[4]/DDR1_DQSP[2]	AT32 M_B_DQSN3	
M_B_DQ45	BA27	DDR1_DQ[61]/DDR1_DQ[45]	DDR1_DQSN[5]/DDR1_DQSN[3]	AR32 M_B_DQSP3	
M_B_DQ46	BA25	DDR1_DQ[62]/DDR1_DQ[46]	DDR1_DQSP[5]/DDR1_DQSP[3]	BA30 M_B_DQSN4	
M_B_DQ47	BB25	DDR1_DQ[63]/DDR1_DQ[47]	DDR0_DQSN[6]/DDR1_DQSN[4]	AY30 M_B_DQSP4	
M_B_DQ48	AU27	DDR1_DQ[48]	DDR0_DQSP[6]/DDR1_DQSP[4]	AY26 M_B_DQSN5	
M_B_DQ49	AT27	DDR1_DQ[49]	DDR0_DQSN[7]/DDR1_DQSN[5]	BA26 M_B_DQSP5	
M_B_DQ50	AT25	DDR1_DQ[50]	DDR0_DQSP[7]/DDR1_DQSP[5]	AR25 M_B_DQSN6	
M_B_DQ51	AU25	DDR1_DQ[51]	DDR1_DQSN[6]	AR27 M_B_DQSP6	
M_B_DQ52	AP27	DDR1_DQ[52]	DDR1_DQSP[6]	AT22 M_B_DQSN7	
M_B_DQ53	AN27	DDR1_DQ[53]	DDR1_DQSN[7]	AR21 M_B_DQSP7	
M_B_DQ54	AN25	DDR1_DQ[54]	DDR1_DQSP[7]		
M_B_DQ55	AP25	DDR1_DQ[55]		AN43	
M_B_DQ56	AT22	DDR1_DQ[56]	DDR1_ALERT#	AP43	
M_B_DQ57	AU22	DDR1_DQ[57]	DDR1_PAR	AT13	SM_DRAMRST#
M_B_DQ58	AU21	DDR1_DQ[58]	DRAM_RESET#	AR18	SM_RCOMP_0 R65 200/F_2
M_B_DQ59	AT21	DDR1_DQ[59]	DDR_RCOMP[0]	AT18	SM_RCOMP_1 R66 80.6/F_2
M_B_DQ60	AN22	DDR1_DQ[60]	DDR_RCOMP[1]	AU18	SM_RCOMP_2 R64 162/F_2
M_B_DQ61	AP22	DDR1_DQ[61]	DDR_RCOMP[2]		
M_B_DQ62	AP21	DDR1_DQ[62]			
M_B_DQ63	AN21	DDR1_DQ[63]			

NIL-DDR CH - B

+1.2VSUS
R69 *0_2 PV

12mils width

*SKL_ULT
REV = 1

QCMC

WWW.AliSaler.Com

NB5	PROJECT : Y0DD Quanta Computer Inc.		
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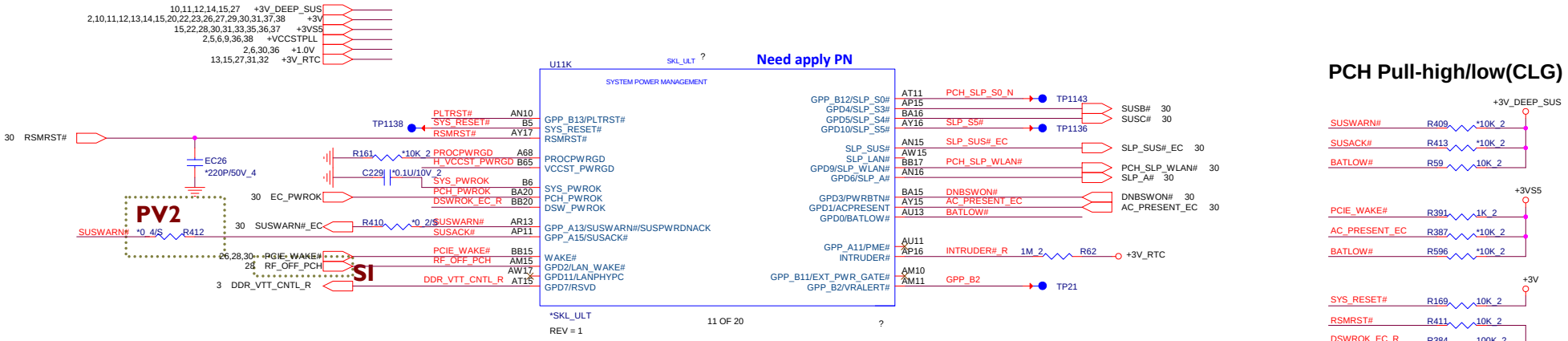
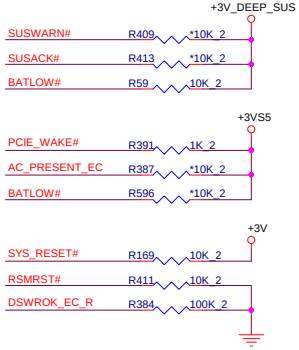
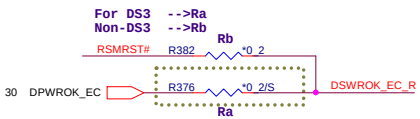


PCH Pull-high/low(CLG)

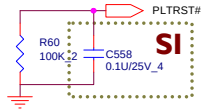


For DS3 Sequence

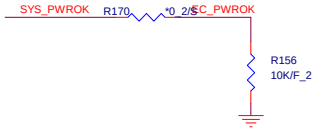


PLTRST#(CLG)

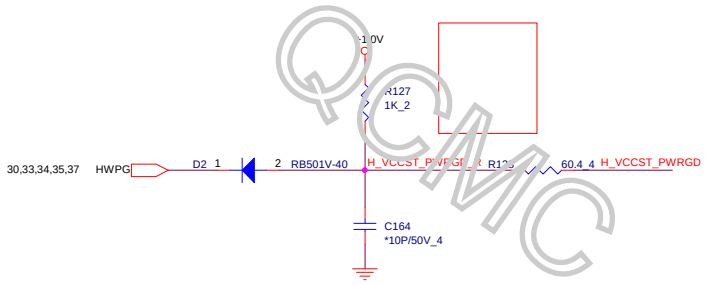
Check Q2010 Rise/Fall time less than 100ns



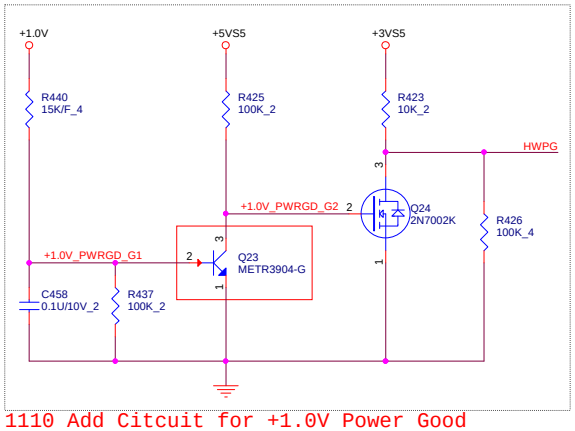
System PWR_OK(CLG)



1211 Del
+VCCSTPLL and R134



R10479 close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



1110 Add Citcuit for +1.0V Power Good

1118 Change Change Q7062 P/N from BA051440000 to BA039040020, Del D7002,D7003, R10526, R10527

QCMC

NB5	PROJECT : Y0DD Quanta Computer Inc.	
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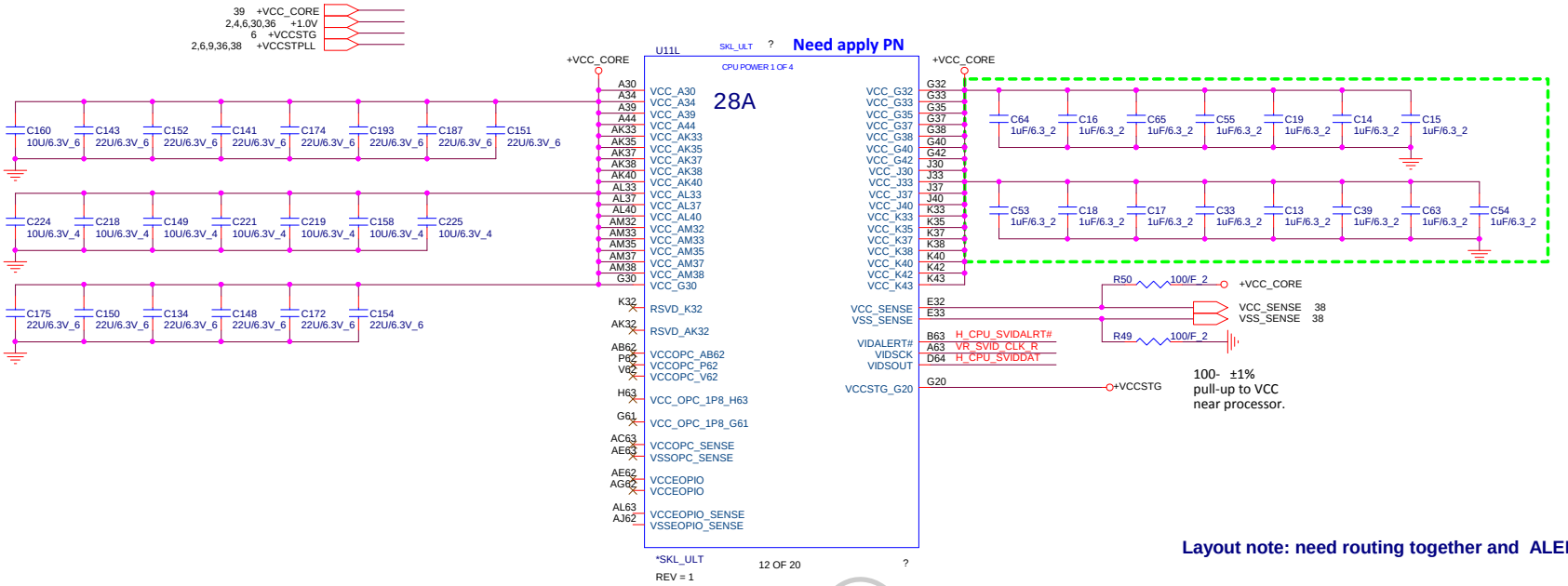
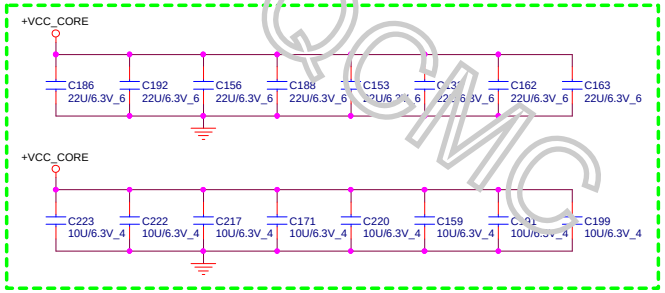
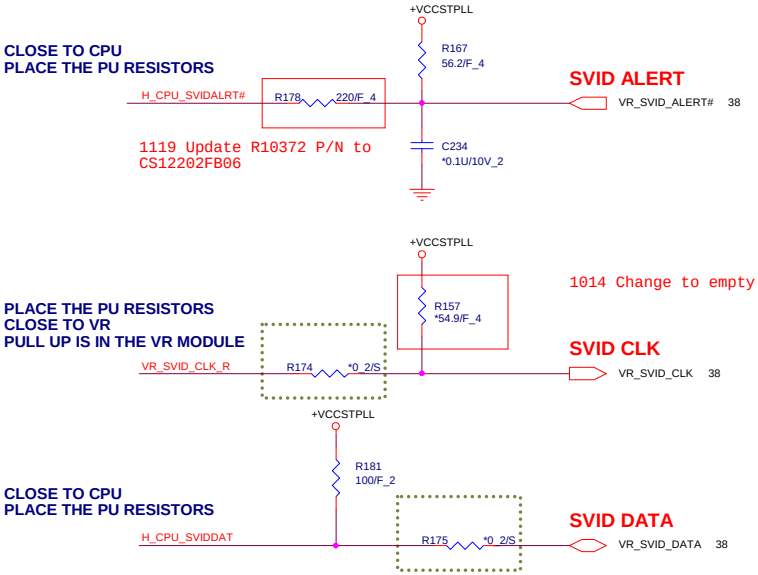


100- ±1% pull-up to VCC near processor.

Close U11



Layout note: need routing together and ALERT need between CLK and DATA.



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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NB5

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Quanta Computer Inc.

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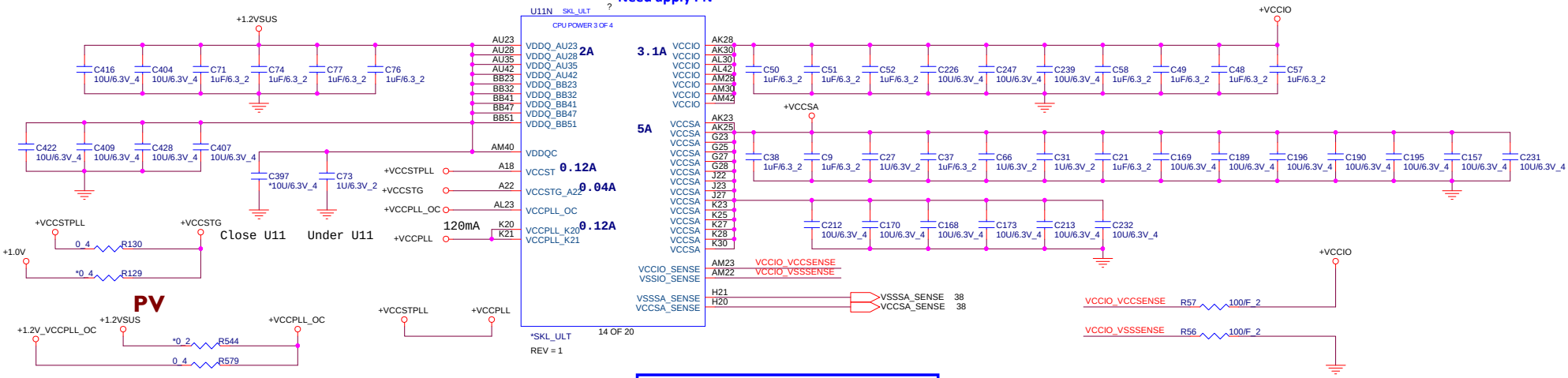
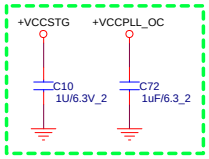
+VCCSTPLL 2,5,9,36,38
+VCCSA 38,39
+1.2VSUS 3,17,18,34,36
+1.0V_DEEP_SUS 9,13,15,35,36
+1.0V 2,4,30,36
+3VPCU 13,15,27,28,30,31,32,33
+1.2V_VCCPLL_OC 36

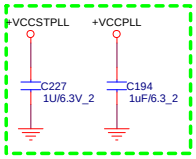
Need apply PN



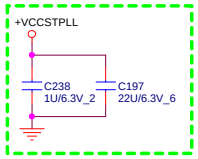
Under U11



Close U11

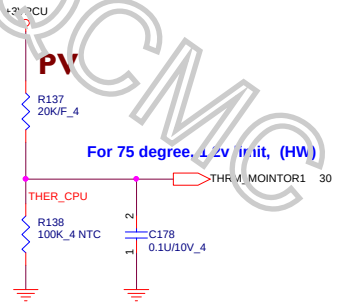


Close A18 Ball



IO Thrm Protect

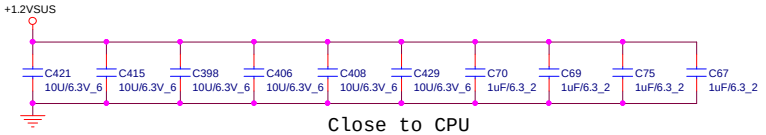
For 65 degree, 1.8v limit, (SW)



For 75 degree, 1.2v limit, (HW)

QCMC

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



Close to CPU

NB5

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Custom	SKL U (5/14)	1A

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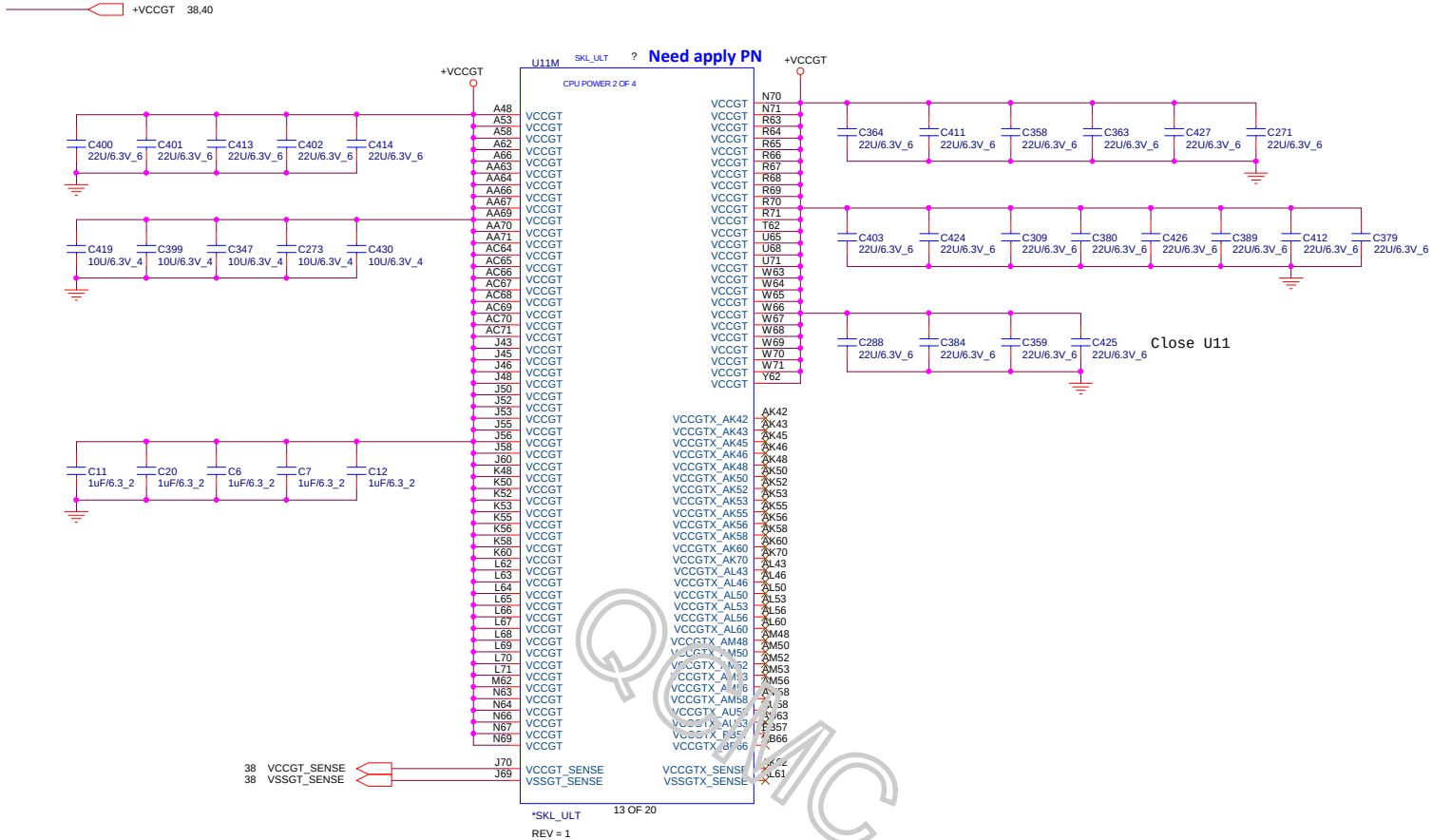
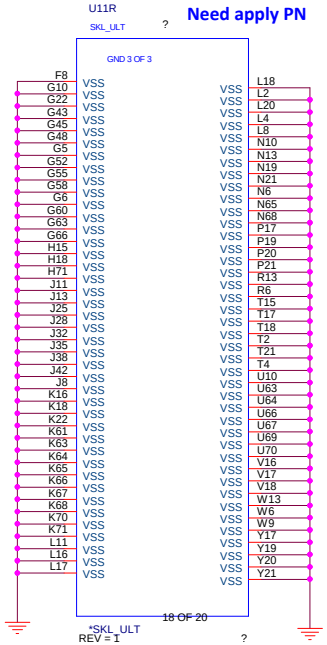
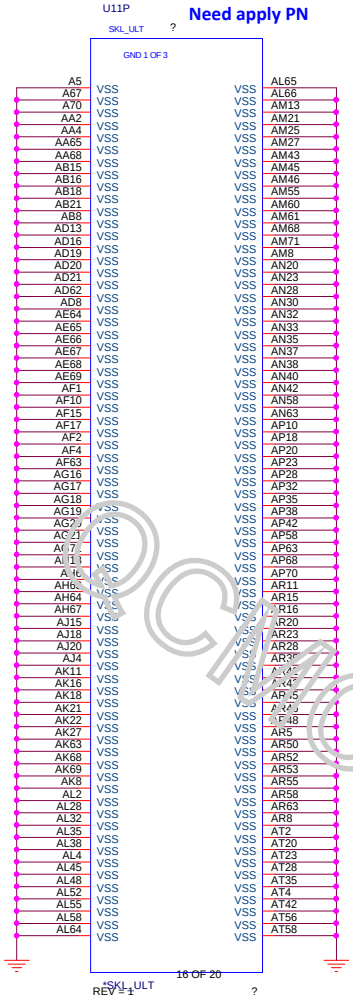
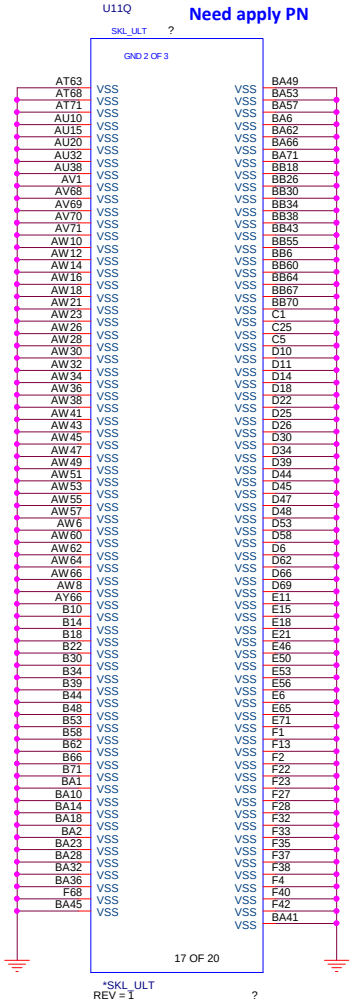


QCOM

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed







QCI

NB5

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SKL U (7/14)	1A

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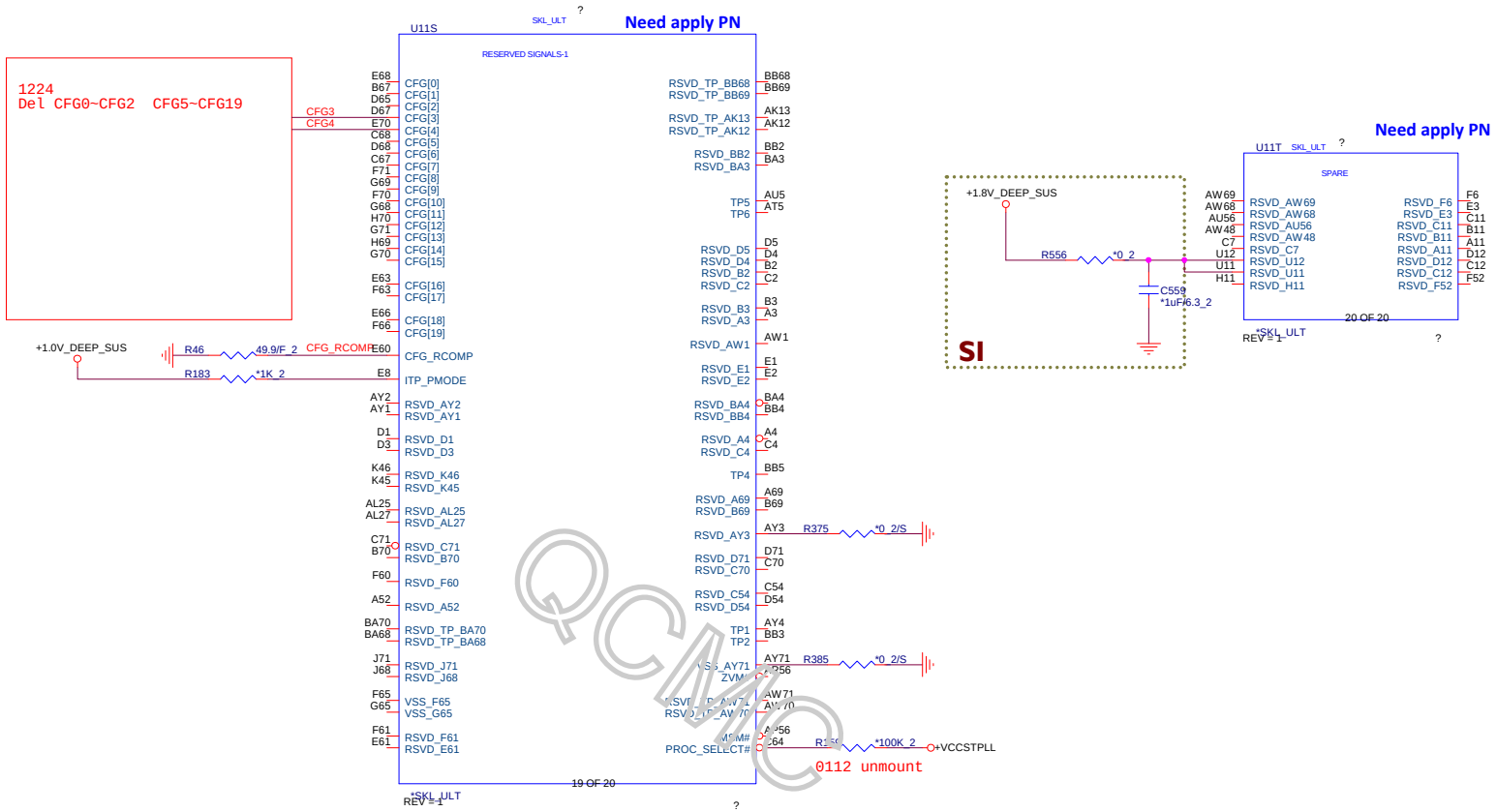

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R143 *1K_2
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R42 1K_2

NB5

PROJECT : Y0DD
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+3V_DEEP_SUS 4,11,12,14,15,27
+3V 2,4,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38
+5V 22,23,24,27,37
+1.0V 2,4,6,30,36
+3VS5 4,15,22,28,30,31,33,35,36,37

Need apply PN

U11E

SKL_ULT

SPI - FLASH

PCH_SPI1_CLK AV2 SPI0_CLK
PCH_SPI1_SO AW3 SPI0_MISO
PCH_SPI1_SI AV3 SPI0_MOSI
PCH_SPI_IO2 AW2 SPI0_IO2
PCH_SPI_IO3 AU4 SPI0_IO3
PCH_SPI_CS0# AU3 SPI0_CS0#
AU2 SPI0_CS1#
AU1 SPI0_CS2#

SPI - TOUCH

TP1137
GPP_D1 M2 GPP_D1/SPI1_CLK
30 SIO_EXT_SMI# SIO_EXT_SMI# M3 GPP_D2/SPI1_MISO
30 PCI_SERR# PCI_SERR# J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

C LINK

Support Vpro
28 CL_CLK G3 CL_CLK
28 CL_DAT G2 CL_DATA
28 CL_RST# G1 CL_RST#

30 EC_RCIN# AW13 GPP_A0/RCIN#
26,30 SERIRQ AY11 GPP_A6/SERIRQ

*SKL_ULT
REV = 1

5 OF 20

SMBUS, SMLINK

GPP_C0/SMBCLK R7 SMB_PCH_CLK
GPP_C1/SMBDATA R8 SMB_PCH_DAT
GPP_C2/SMBALERT# R10 SML0ALERT# 11
GPP_C3/SML0CLK R9 SMB_ME0_CLK
GPP_C4/SML0DATA W2 SMB_ME0_DAT
GPP_C5/SML0ALERT# W1 SML1ALERT# 11
GPP_C6/SML1CLK W3 SMB_ME1_CLK
GPP_C7/SML1DATA V3 SMB_ME1_DAT
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23 TP15

LPC

GPP_A1/LAD0/ESPI_IO0 AY13 LAD0 26,28,30
GPP_A2/LAD1/ESPI_IO1 BA13 LAD1 26,28,30
GPP_A3/LAD2/ESPI_IO2 BB13 LAD2 26,28,30
GPP_A4/LAD3/ESPI_IO3 AY12 LAD3 26,28,30
GPP_A5/LFRAME#/ESPI_CS# BA12 LFRAME# 26,28,30
GPP_A14/SUS_STAT#/ESPI_RESET# BA11

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 CLK_PCI_EC_R
GPP_A10/CLKOUT_LPC1 AY9 CLK_PCI_LPC_R
GPP_A8/CLKRUN# AW11 CLKRUN# CLKRUN# 30

R408 22/F_4
R404 22/F_4
R405 0_4

EC25 18P/50V_4
CLK_24M_KBC 30
CLK_24M_DEBUG 28
EMI(near PCH)
EC24 18P/50V_4
CLK_PCI_TPM 26
EC23 18P/50V_4
EMI(near PCH)

MV

GPIO Pull UP

+3V
SERIRQ R377 10K_2
CLKRUN# R380 8.2K/F_4
SIO_EXT_SMI# R205 10K_2
EC_RCIN# R378 10K_2
PCI_SERR# R202 10K_2

+3V_DEEP_SUS
27 SMB_PCH_CLK R360 2.2K_2
27 SMB_PCH_DAT R366 2.2K_2
SMB_ME0_CLK R232 499/F_4
SMB_ME0_DAT R257 499/F_4
SMB_ME1_CLK R341 1K_2
SMB_ME1_DAT R333 1K_2
12 ACC_LED# R173 10K_2

SI

SMBus/Pull-up(CLG)

1230
Change net name from SMB_RUN_CLK to SMB_PCH_CLK
Change net name from SMB_RUN_DAT to SMB_PCH_DAT

Touch Pad
XDP

PCH SPI ROM(CLG)

Vendor	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		[illegible]S023

Quanta

4M SPI ROM Socket

+3VSPI
30 PCH_SPI_CS0#_R PCH_SPI_CS0#_R
30 PCH_SPI1_CLK_R PCH_SPI1_CLK_R
30 PCH_SPI1_SI_R PCH_SPI1_SI_R
30 PCH_SPI1_SO_R PCH_SPI1_SO_R
BIOS_WP#
HOLD#

SI

U23&U24 footprint 要重疊

TP65 PCH_SPI_CS0#_R
TP68 PCH_SPI1_CLK_R
TP71 PCH_SPI1_SI_R
TP67 PCH_SPI1_SO_R
TP70 BIOS_WP#
TP66 HOLD#
TP66-71 need place to TOP

PCH SPI ROM(CLG)

15 +3V_M

+3V_M
U17
PCH_SPI_CS0# R340 15/F_4 PCH_SPI_CS0#_R 1 CE# VDD 8 +3VSPI
PCH_SPI1_CLK R361 15/F_4 PCH_SPI1_CLK_R 6 SCK
PCH_SPI1_SI R367 15/F_4 PCH_SPI1_SI_R 5 SI
PCH_SPI1_SO R354 15/F_4 PCH_SPI1_SO_R 2 SO HOLD# 7 HOLD# R343 1K_4
WP# 3 VSS 4 R342 15/F_4
GD25B64BSIGR
AKE3EFP0N07
R457/R453/R450/R451/R546/R548 close to U15 pin
C373 22P/50V_4
C346 0.1U/10V_4
C376 1U/10V_4 +3VSPI R359 1K_4
PCH_SPI_IO2 R365 15/F_4 BIOS_WP#
PCH_SPI_IO3

NB5

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Quanta Computer Inc.

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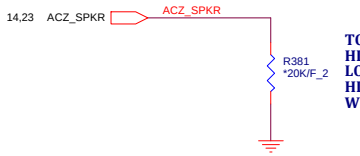
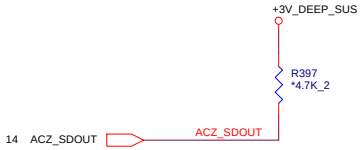
Functional Strap Definitions

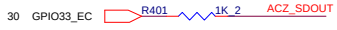
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



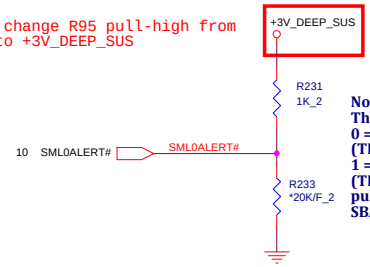
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



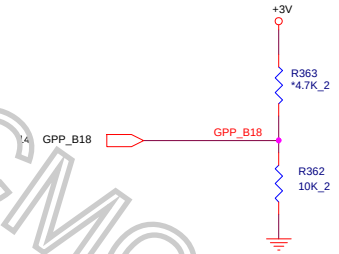
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



1212 change R95 pull-high from +3V to +3V_DEEP_SUS



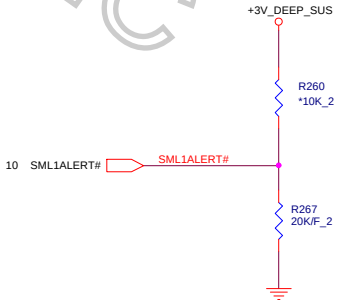
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

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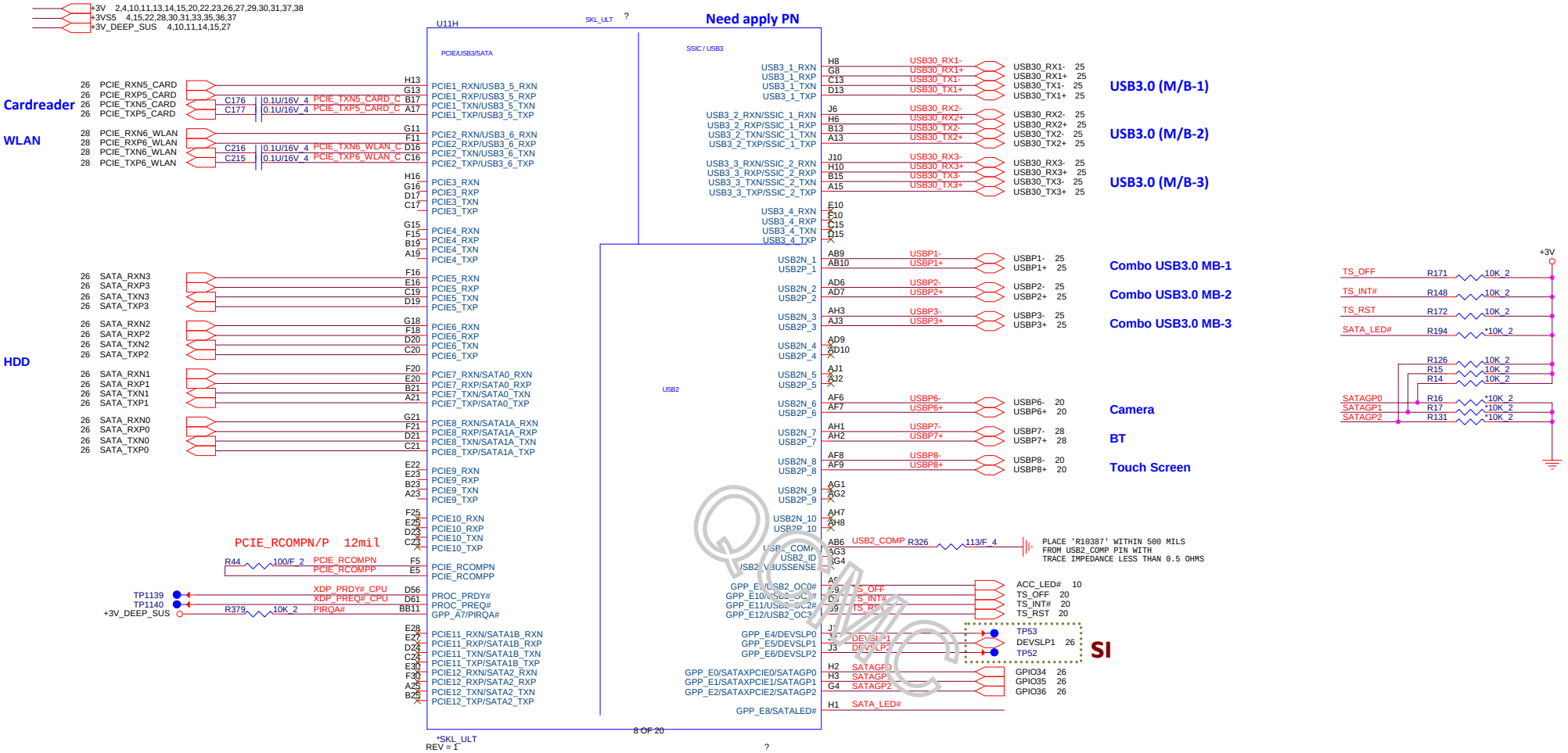

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	CardReader	Port0	Un-used
Port2	WLAN	Port1	CardReader
Port3	Un-used	Port2	WLAN
Port4	Un-used	Port3	Un-used
Port5	SSD	Port4	Un-used
Port6	SSD	Port5	SSD
Port7	SSD		
Port8	SSD		
Port9	Un-used		
Port10	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	Sensor Hub
PORT-5	NC
PORT-6	Camera
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

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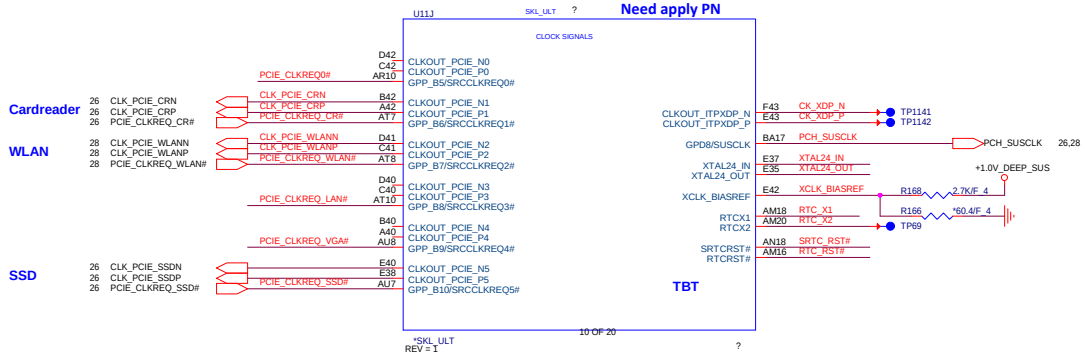
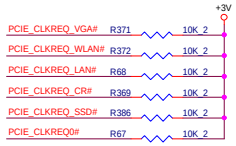
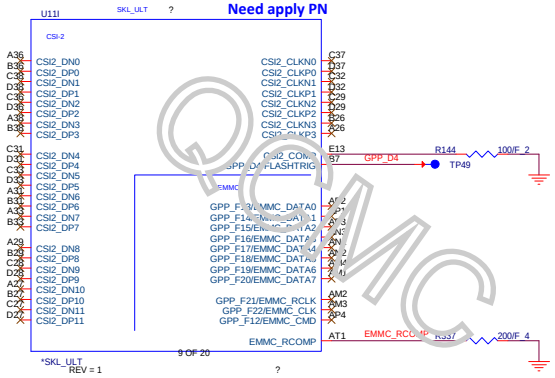
+1.8V_DEEP_SUS 9,15,35,37
+3V 2,4,10,11,12,14,15,20,22,23,26,27,29,30,31,37,38



CLK_REQ/Strap Pin(CLG)





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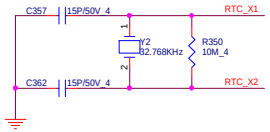
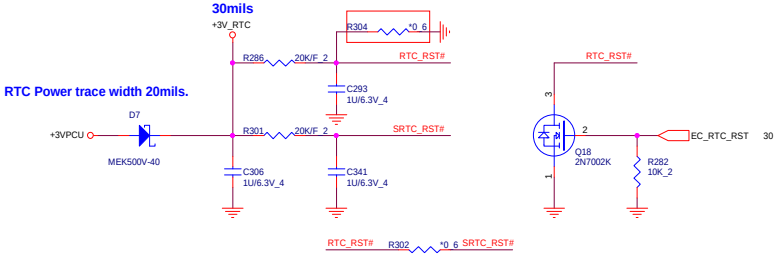
RTC Clock 32.768KHz

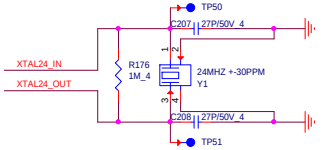


RTC Circuitry(RTC)

+3V_RTC 4,15,27,31,32
+3VPCU 6,15,27,28,30,31,32,33



External Crystal



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Skylake (GPIO)

+3V 2,4,10,11,12,13,15,20,22,23,26,27,29,30,31,37,38
+3V_DEEP_SUS 4,10,11,12,15,27

BT_OFF R219 10K_2 +3V_DEEP_SUS
PCH_TEMPALERT# R249 10K_2
SIO_EXT_SCI# R338 10K_2
ACCEL_INTA# R327 *10K_2
UART2_RXD R306 49.9K_4
UART2_TXD R314 49.9K_4

1227 Add R306 and R314 for UART2 function reserved

11 GPP_B18
11 GSPI1_MOSI
25 UART2_RXD
25 UART2_TXD
30 SIO_EXT_SCI#

TP18 GPP_B15 AN8
TP30 GPP_B16 AP7
TP33 GPP_B17 AP8
GPP_B18 AR7
TP25 GPP_B19 AM5
TP27 GPP_B20 AN7
TP29 GPP_B21 AP5
GSPI1_MOSI AN5
TP64 GPP_C8 AB1
TP62 GPP_C9 AB2
TP61 GPP_C10 W4
TP12 GPP_C11 AB3
UART2_RXD AD1
UART2_TXD AD2
ACCEL_INTA# AD3
SIO_EXT_SCI# AD4
TP9 I2C1_SDA U7
TP10 I2C1_SCL U6
U8
U9
AH9
AH10
AH11
AH12
AF11
AF12

U11F SKL_ULT ? Need apply PN

LPSS
GPP_B15/GSPI0_CS#
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B18/GSPI0_MOSI
GPP_B19/GSPI1_CS#
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_B22/GSPI1_MOSI
GPP_C8/UART0_RXD
GPP_C9/UART0_TXD
GPP_C10/UART0_RTS#
GPP_C11/UART0_CTS#
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#
GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL
GPP_F4/I2C2_SDA
GPP_F5/I2C2_SCL
GPP_F6/I2C3_SDA
GPP_F7/I2C3_SCL
GPP_F8/I2C4_SDA
GPP_F9/I2C4_SCL

ISH
GPP_D9 P2
GPP_D10 P3
GPP_D11 P4
GPP_D12 P1
GPP_D5/ISH_I2C0_SDA M4
GPP_D6/ISH_I2C0_SCL N3
GPP_D7/ISH_I2C1_SDA N1
GPP_D8/ISH_I2C1_SCL N2
GPP_F10/I2C5_SDA/ISH_I2C2_SDA AD11
GPP_F11/I2C5_SCL/ISH_I2C2_SCL AD12
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA U1
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL U2
GPP_D15/ISH_UART0_RTS# U3
GPP_D16/ISH_UART0_CTS#/SML0BALERT# U4
GPP_C12/UART1_RXD/ISH_UART1_RXD AC1
GPP_C13/UART1_TXD/ISH_UART1_TXD AC2
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AC3
GPP_C15/UART1_CTS#/ISH_UART1_CTS# AB4
GPP_A18/ISH_GP0 AY8
GPP_A19/ISH_GP1 BA8
GPP_A20/ISH_GP2 BB7
GPP_A21/ISH_GP3 BA7
GPP_A22/ISH_GP4 AY7
GPP_A23/ISH_GP5 AW7
GPP_A12/BM_BUSY#/ISH_GP6 AP13

GPP_D9 TP76
GPP_D10 TP77
BT_OFF 28
ISH_I2C0_SDA 29
ISH_I2C0_SCL 29
ISH_I2C2_SDA TP14
ISH_I2C2_SCL TP11
PCH_TEMPALERT# TP59
SML0BDATA TP58
SML0BCLK TP57
SML0BALERT# TP60
UART1_RXD TP19
UART1_TXD TP20
UART1_RTS TP23
UART1_CTS TP17
COOL SENSE
ISH_GYRO_DRDY 29
ISH_GYRO_INT 29
ISH_AE_INT 29
ISH_ACC_INT 29
DISABLE KB 29
GPP_A12

*SKL_ULT
REV = 1
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+3V
COOL SENSE R2 *10K_2
ISH_GYRO_DRDY R9 *10K_2
ISH_GYRO_INT R7 10K_2
ISH_AE_INT R5 10K_2
ISH_ACC_INT R3 10K_2
DISABLE KB R1 10K_2
GPP_A12 R414 *10K_2
R8 *10K_2
R6 *10K_2
R4 *10K_2
ISH_I2C0_SDA R210 10K_2
ISH_I2C0_SCL R212 10K_2
ISH_I2C2_SDA R53 10K_2
ISH_I2C2_SCL R52 10K_2
R585 *10K_2 +3V_DEEP_SUS
D14 RB500V-40 EMU_LID 20,30

PV2

R311 10K_2 BOARD_ID0 R313 *10K_2 +3V_DEEP_SUS
R307 10K_2 BOARD_ID1 R322 *10K_2
R315 10K_2 BOARD_ID2 R328 *10K_2
R274 10K_2 BOARD_ID3 R275 *10K_2
R289 10K_2 BOARD_ID4 R273 *10K_2
R291 10K_2 BOARD_ID5 R288 *10K_2
R290 *10K_2 BOARD_ID6 R303 10K_2
R317 10K_2 BOARD_ID7 R316 *10K_2
R392 *10K_2 BOARD_ID8 R396 10K_2

HDA Bus(CLG)

+3V_DEEP_SUS R390 *1K_4 ACZ_SYNC
23 ACZ_SYNC_AUDIO R394 33_4 ACZ_SYNC
23 ACZ_RST#_AUDIO R388 33_4 ACZ_RST#
ACZ_SDOUT_AUDIO R400 33_4 ACZ_SDOUT
R402 33_4 ACZ_BCLK
C423

U11G SKL_ULT ? Need apply PN

AUDIO
11 ACZ_SDOUT ACZ_SYNC BA22
23 ACZ_SDIN0 ACZ_BCLK AY22
ACZ_SDOUT BB22
ACZ_SDIN0 BA21
AY21
ACZ_RST# AW22
J5
AY20
AW20
HDA_SYNC/I2S0_SFRM
HDA_BLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_RST#/I2S1_SCLK
GPP_D23/I2S_MCLK
I2S1_SFRM
I2S1_TXD
TP22 SSP2_SFRM AK7
TP16 SSP2_SCLK AK6
TP13 SSP2_TXD AK9
TP26 SSP2_RXD AK10
GPP_F1/I2S2_SFRM
GPP_F0/I2S2_SCLK
GPP_F2/I2S2_TXD
GPP_F3/I2S2_RXD
TP7 GPP_D19 H5
TP44 GPP_D20 D7
GPP_D19/DMIC_CLK0
GPP_D20/DMIC_DATA0
TP48 GPP_D17 D8
TP43 GPP_D18 C8
GPP_D17/DMIC_CLK1
GPP_D18/DMIC_DATA1
11,23 ACZ_SPKR ACZ_SPKR AW5
GPP_B14/SPKR

SDIO/SDXC
GPP_G0/SD_CMD AB11 BOARD_ID0
GPP_G1/SD_DATA0 AB13 BOARD_ID1
GPP_G2/SD_DATA1 AB12 BOARD_ID2
GPP_G3/SD_DATA2 W12 BOARD_ID3
GPP_G4/SD_DATA3 W11 BOARD_ID4
GPP_G5/SD_CD# W10 BOARD_ID5
GPP_G6/SD_CLK W8 BOARD_ID6
GPP_G7/SD_WP W7 BOARD_ID7
GPP_A17/SD_PWR_EN#/ISH_GP7 BA9 BOARD_ID8
GPP_A16/SD_1P8_SEL BB9
SD_RCOMP AB7 R54 200/F_2
GPP_F23 AF13

*SKL_ULT
REV = 1
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CN1
1 ISH_I2C0_SCL
2 ISH_I2C0_SDA
3 ISH_I2C1_SCL
4 ISH_I2C1_SDA
5
6 ISH_GYRO_DRDY
7 ISH_GYRO_INT
8 ISH_AE_INT
9 ISH_ACC_INT
10
11 COOL SENSE
12 DISABLE KB
13
14 TP5
15 TP3
16 TP2
17 TP1 +3V
18
*ACES_88511-180N

1207
Add Sensors Debug CONN

1209
Change CN5012 footprint from 88511-180n-18p-l to fg-12x59-20-18p

Model	BOARD_ID8	BOARD_ID7	BOARD_ID6	Board ID [5]	BOARD_ID[4:0]
Y0DD	0:VPRO 1:non-VPRO	0:2+2 CPU 1:2+3E CPU	0:ESH 1:ISH	Reserve (Default = 0)	00000:H9CCNNNBKTMLBR-NTD Hynix 4G 1600 00010:EDFA164A2MA-GD-F ELPIDA 4G 1600 00100:K3QF2F20EM-AGCF Samsung 4G 1866 00110: Hynix 4G 1866 01000:ELPIDA 4G 1866 00001:H9CCNNNCPTMLBR-NTD Hynix 8G 1600 00011:EDFB164A1MA-GD-F Micron 8G 1600 00101: Samsung 8G 1866 00111:H9CCNNNCPTMLBR-NUD Hynix 8G 1866 01001: ELPIDA 8G 1866 10000:32bit Hynix 8G 10001:32bit Micron 8G 10010: 32bit Samsung 8G 10011:32bit Hynix 16G 10100: 32bit Micron 16G 10101: 32bit Samsung 16G

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4,10,11,12,14,27 +3V_DEEP_SUS
9,13,35,36 +1.0V_DEEP_SUS
9,35,37 +1.8V_DEEP_SUS
4,13,27,31,32 +3V_RTC
4,22,28,30,31,33,35,36,37 +3VSS
10 +3V_M

U11O SKL_ULT CPU POWER 4 OF 4

Need apply PN

PCH Internal VRM

C820 and C690 close to cpu less then 100 mils

PV

*SKL_ULT
REV = 1

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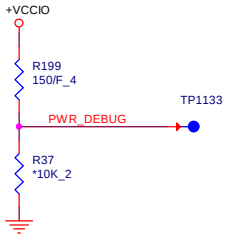

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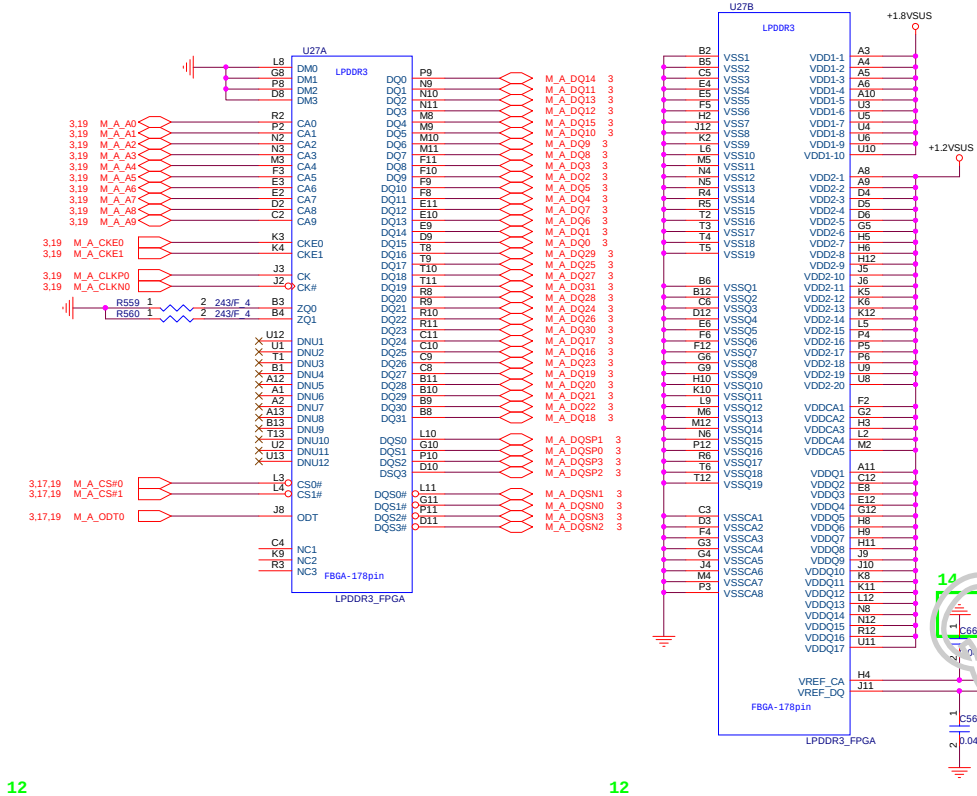
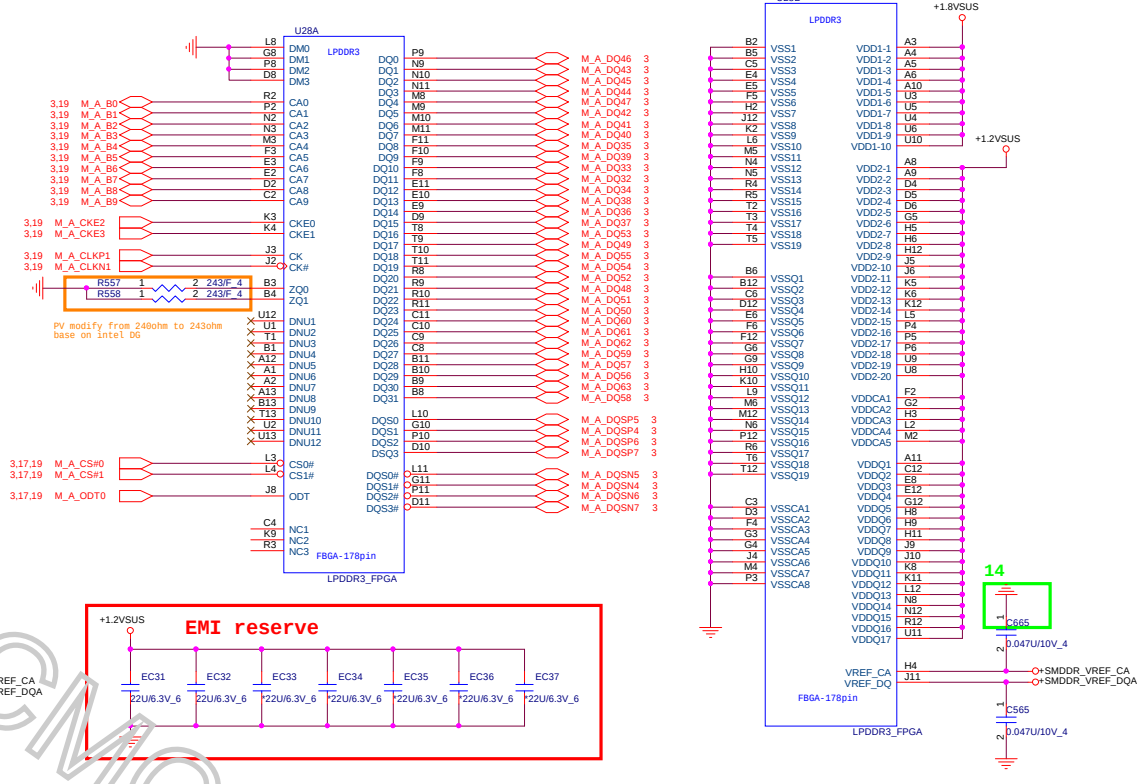
CHANNEL A:8Gb*2 LPDDR3

bit:0-31



bit:32-63

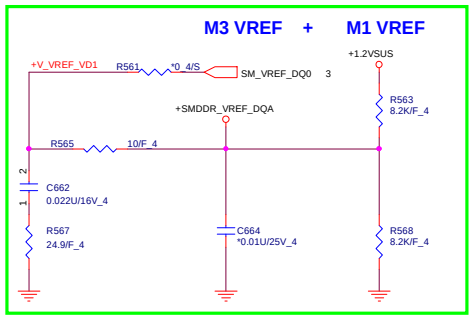


@CMC

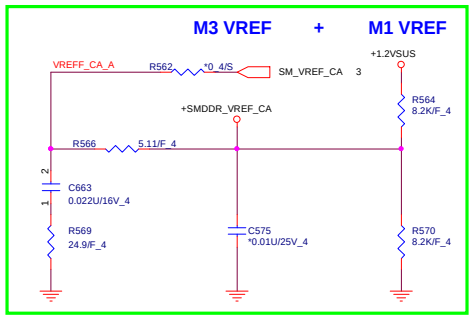
EMI reserve

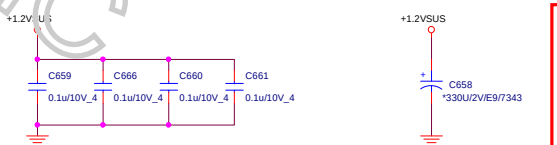
M3 VREF + M1 VREF

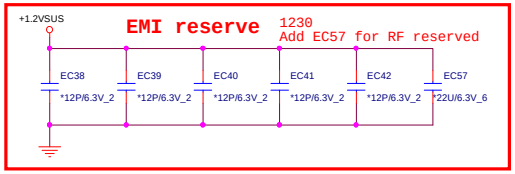
12

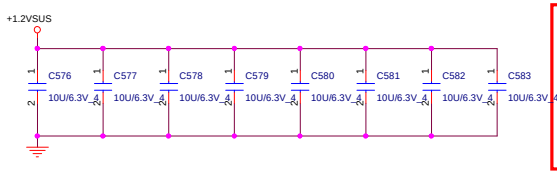


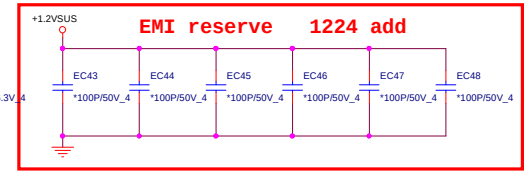
12

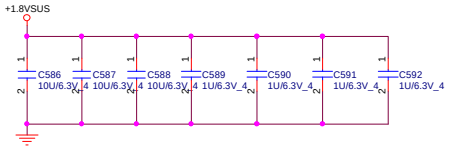


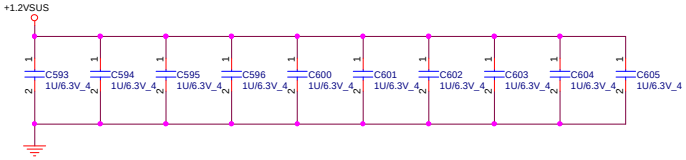


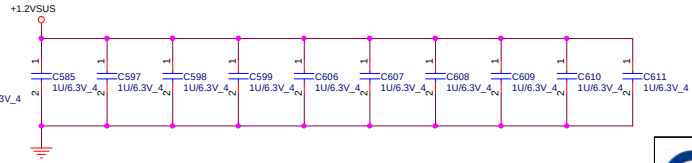












NB5

PROJECT : Y0DD
Quanta Computer Inc.

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	LPDDR3 A	1A

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CHANNEL B:8Gb*2 LPDDR3

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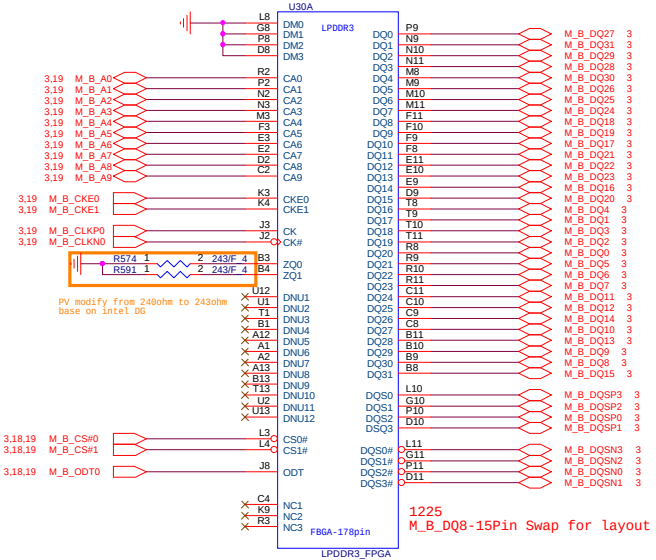

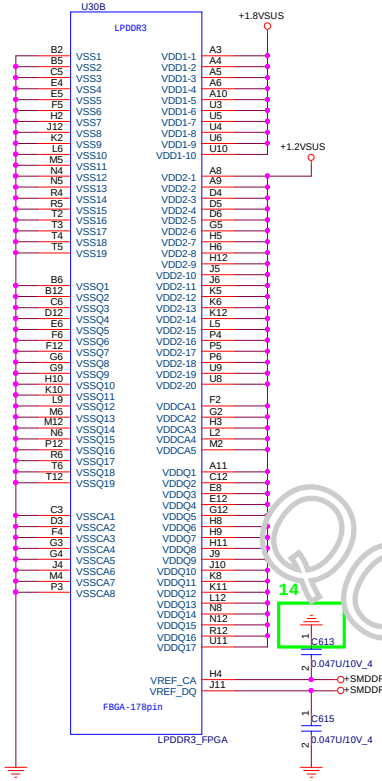

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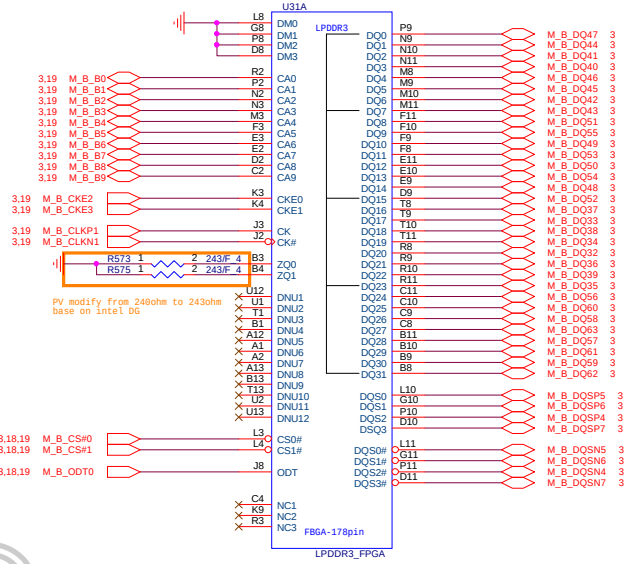

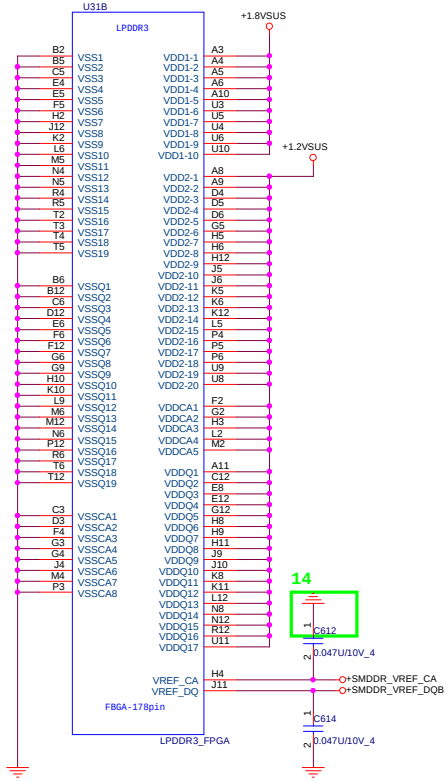

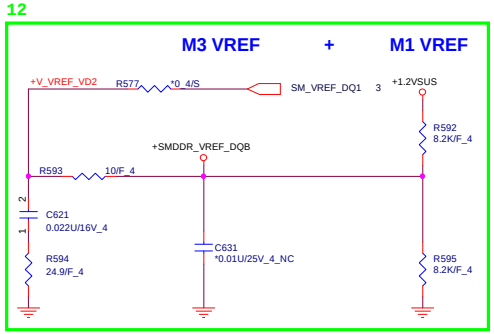

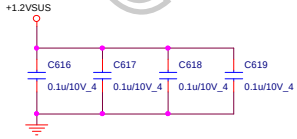

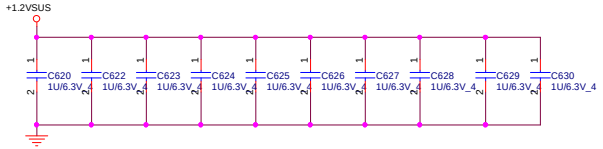

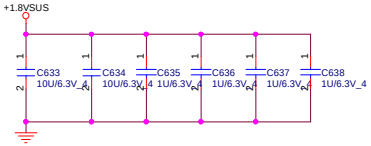

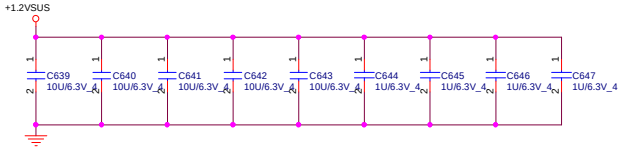

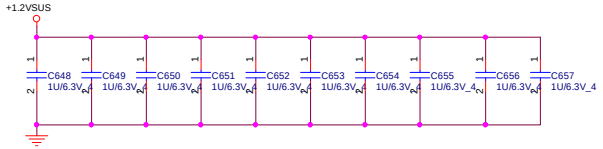

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NB5	PROJECT : Pegasus Quanta Computer Inc.	
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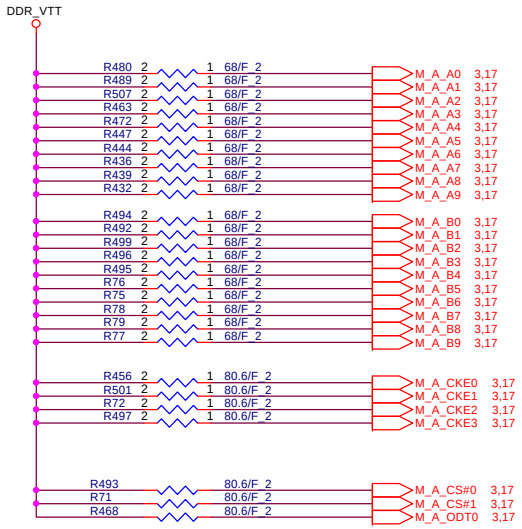

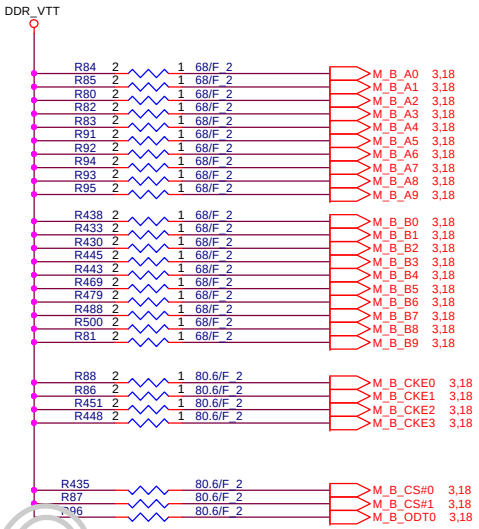

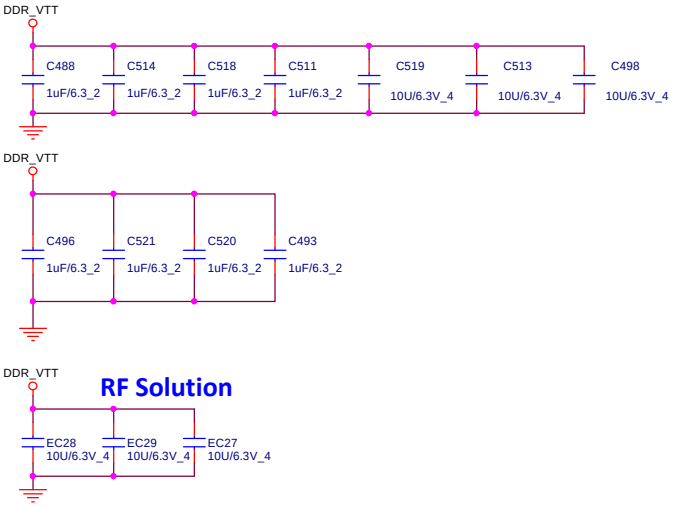

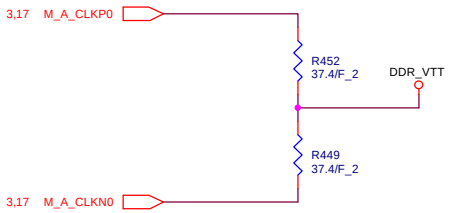

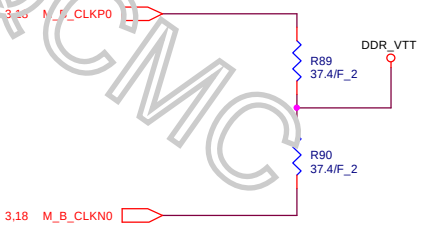

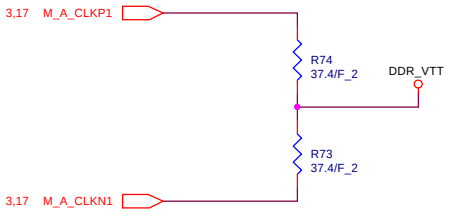

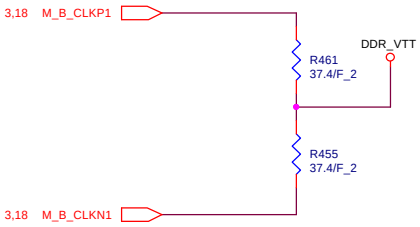

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NB5

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Quanta Computer Inc.

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Custom	LPDDR3 TERMINATION	1A

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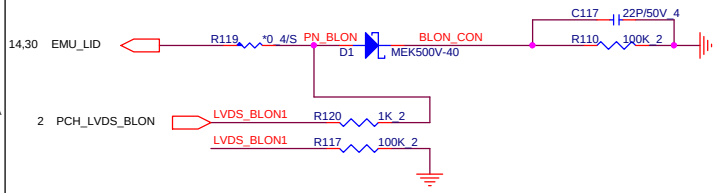
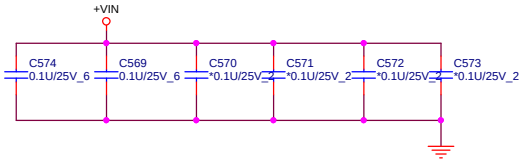
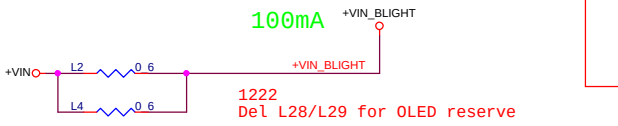
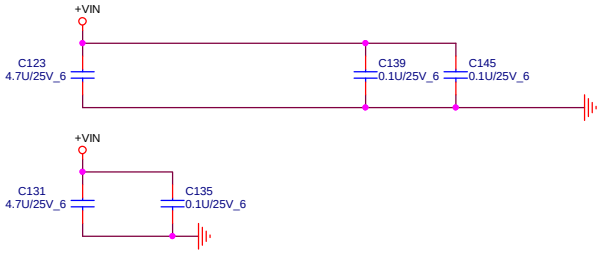
LID Switch

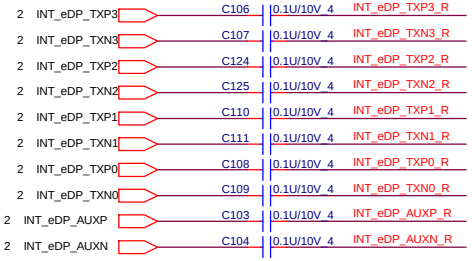




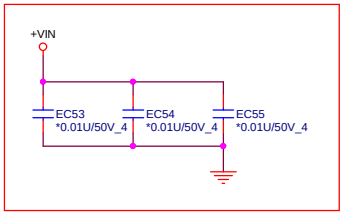


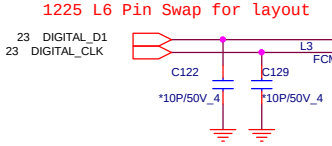
1222
Del L28/L29 for OLED reserve



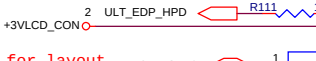


Add EC53, EC54, EC55 for EMI





1225 L6 Pin Swap for layout



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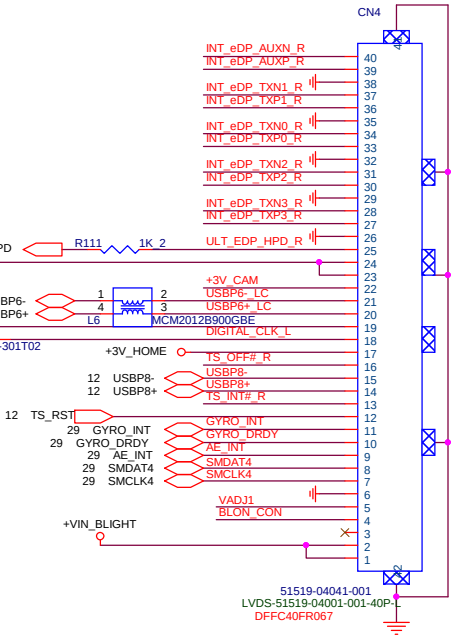
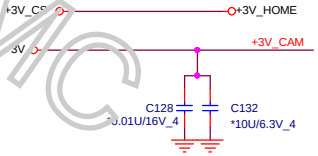
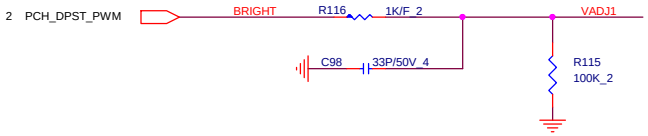
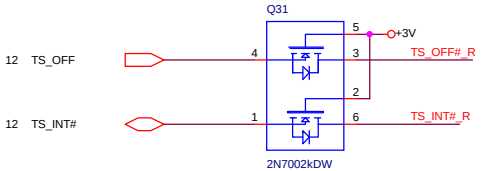
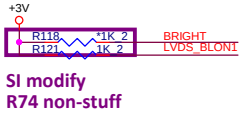


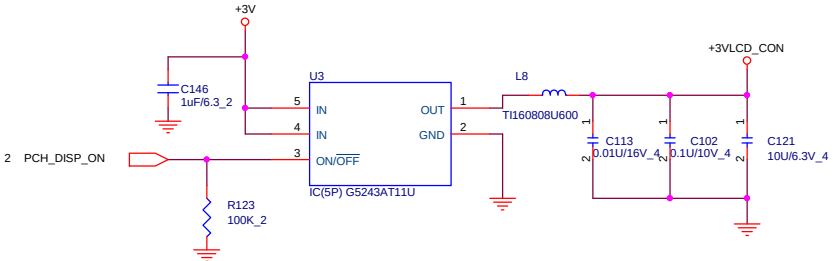








SI modify
R74 non-stuff



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6,13,15,27,28,30,31,32,33 +3VPCU
22,23,24,27,37 +5V
27,32,33,34,35,38,39,40 +VIN

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NB5

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Quanta Computer Inc.

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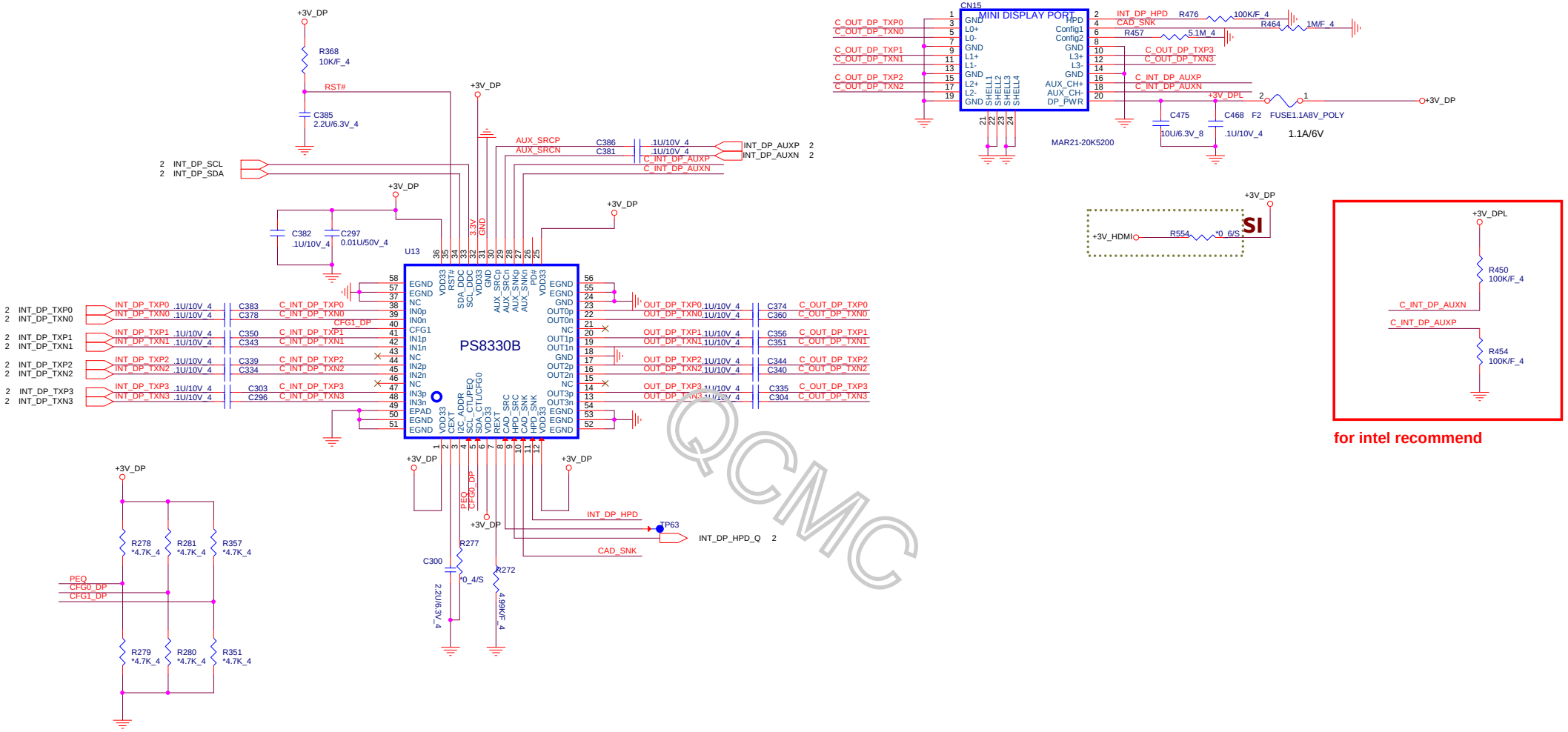
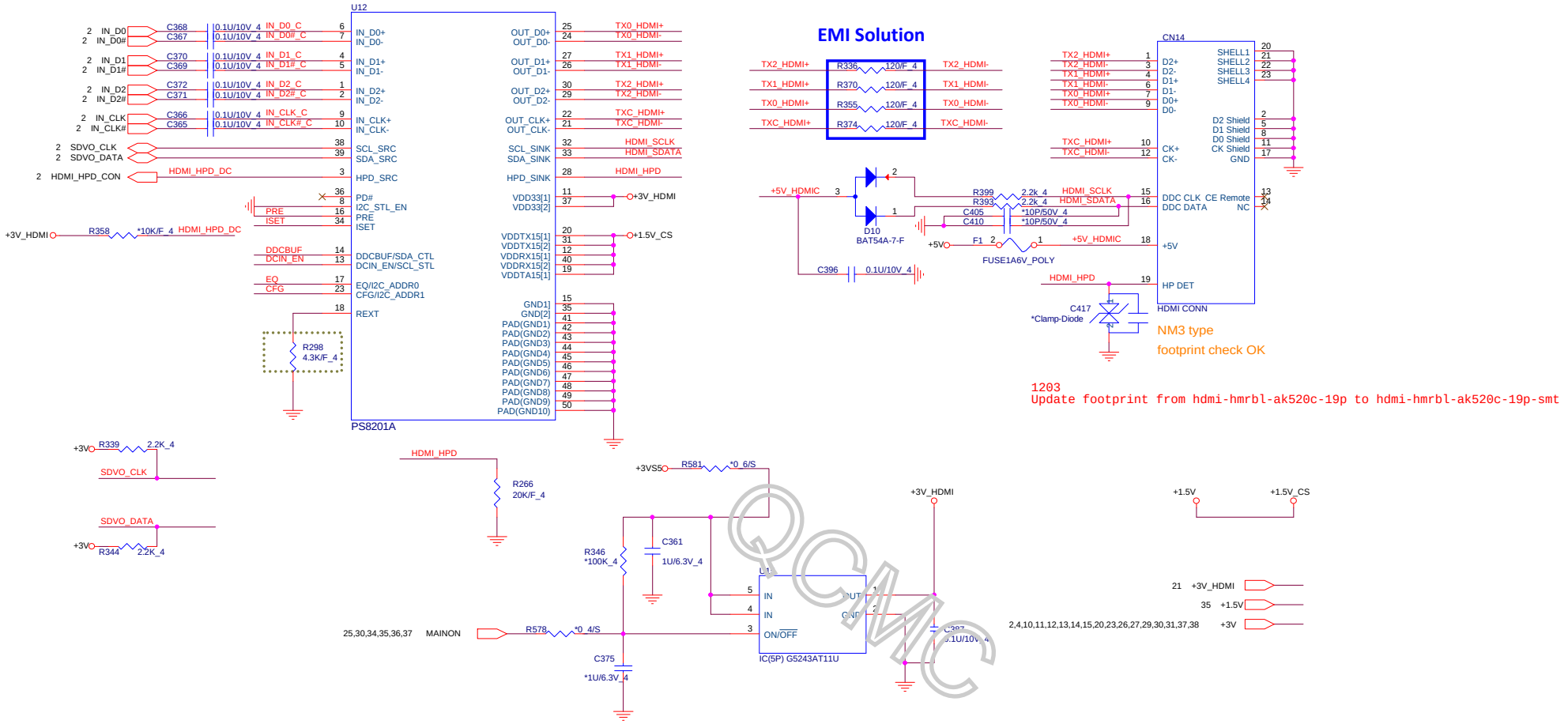
Mini Display

+5V 22,23,24,27,37
+3V 2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38



QCMC

NB5	PROJECT : Y0DD Quanta Computer Inc.	
Size: Custom	Document Number: Re-driver RS8330B	Rev: 1A
Date: Wednesday, January 06, 2016	Sheet 21 of 41	



QCMC

NB5	PROJECT : Y0DD Quanta Computer Inc.		
	Size: Custom	Document Number: HDMI	Rev: 1A
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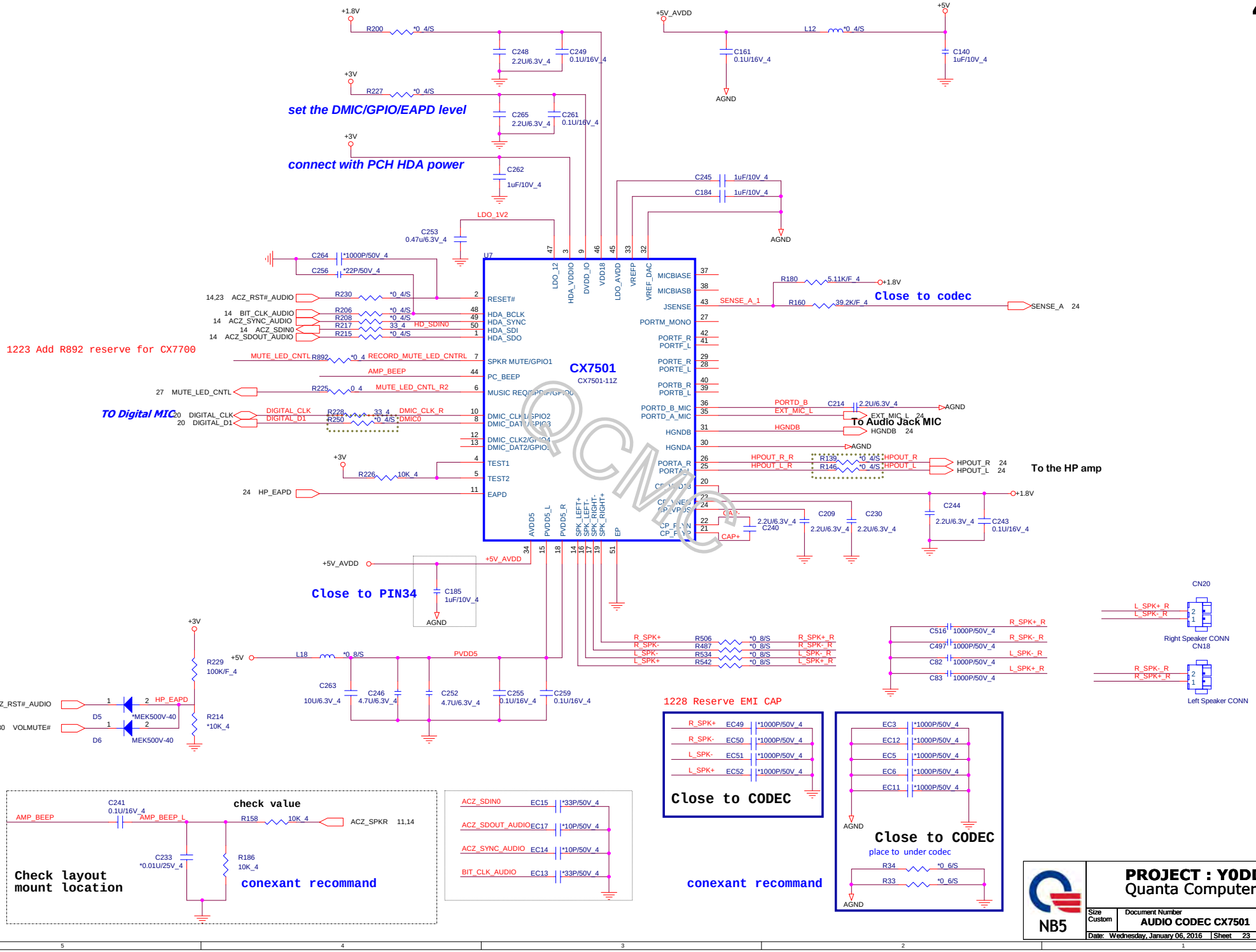

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Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: AUDIO CODEC CX7501
Rev: 1A	
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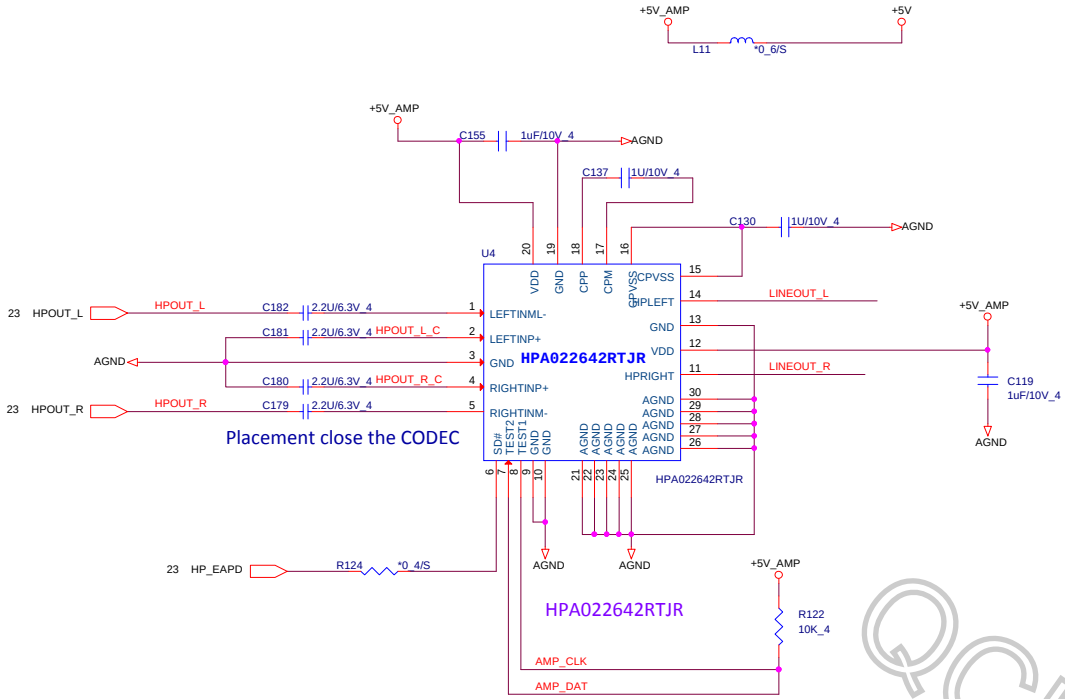
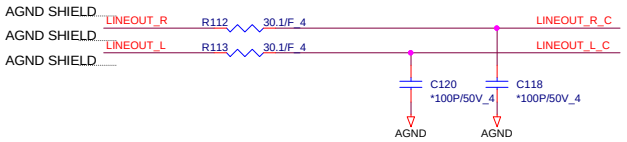
Head Phone out

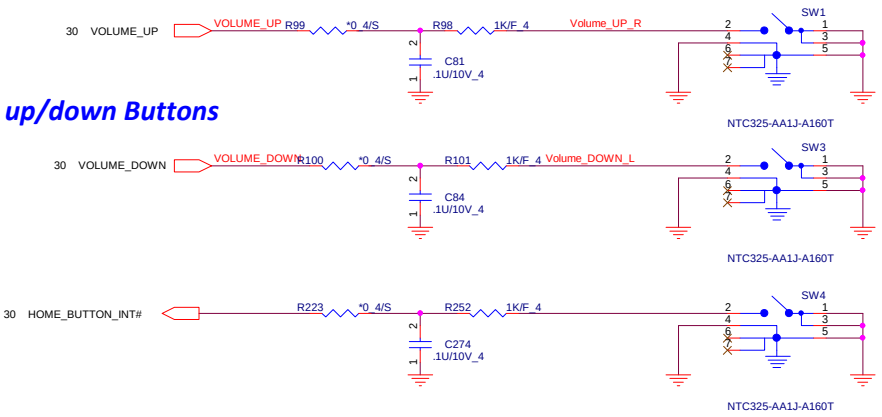




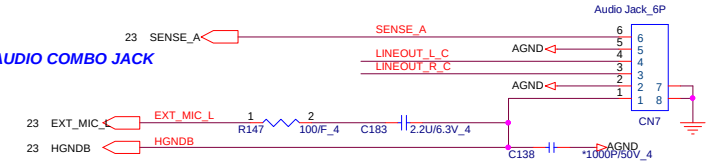
QCMC

Audio combo JACK & Volume up/down Button

Volume up/down Buttons

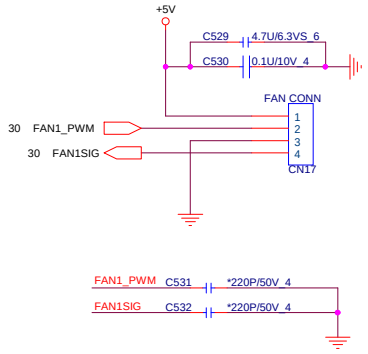


AUDIO COMBO JACK



FAN

1203
Update footprint from 88266-0400-4p-l to 88266-04xl-4p-l-smt



2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38 +3V
22,23,27,37 +5V
4,25,33,34,35,36,37,38,39,40 +5VS

NB5

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Quanta Computer Inc.

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Custom	AUDIO AMP	1A

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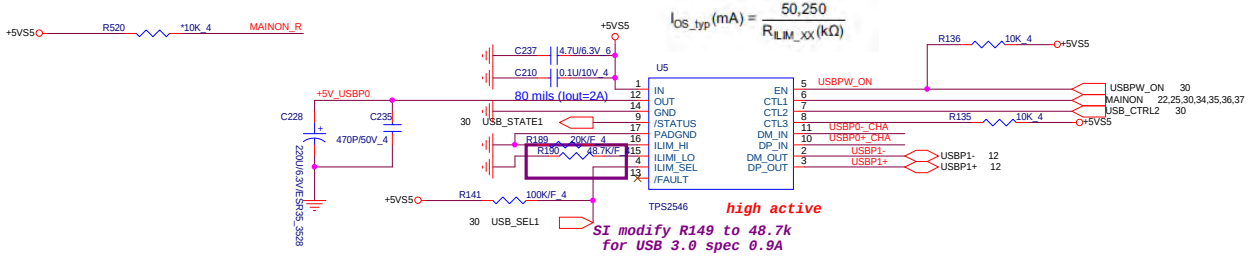
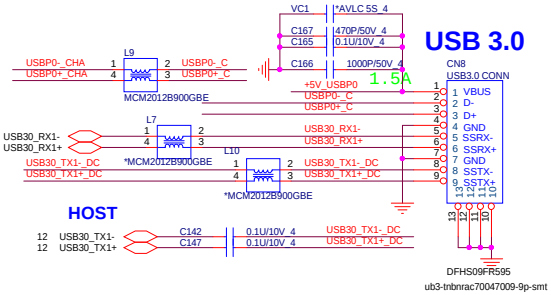
Right side USB 2.0/3.0 Combo

PV ADD R554/R555/R556 10k for USB 3.0 PU





Y11 type

1203
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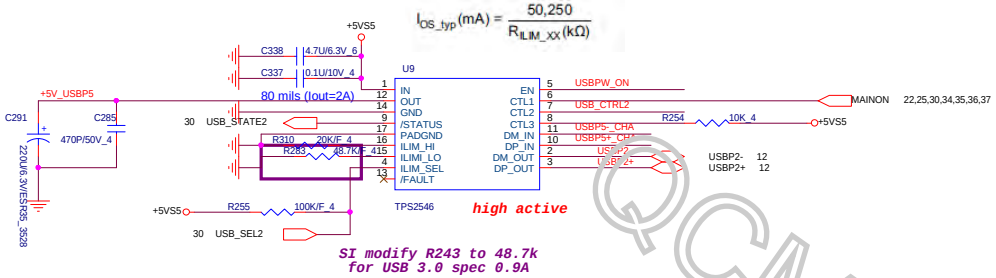
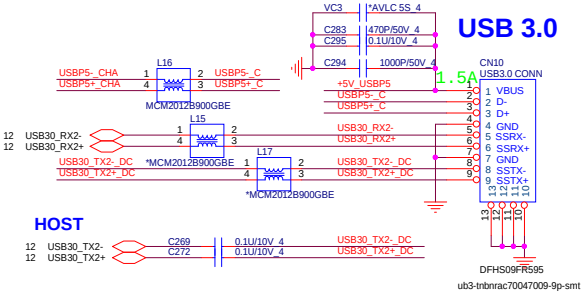
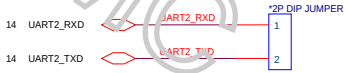
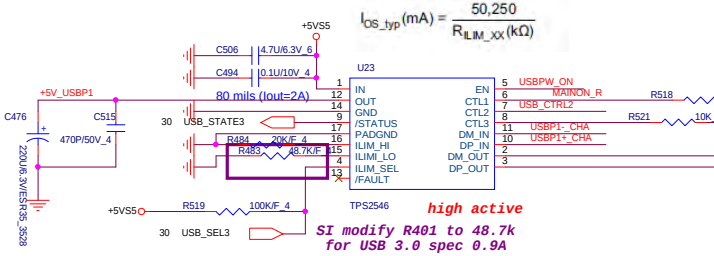




W81 UART



Left side USB 2.0/3.0 Combo



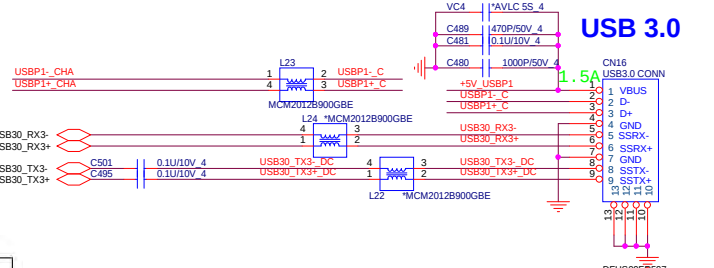


Table 3. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2546 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds	0	0	1	1	ILIM_HI
S3/S4/S5	Auto mode, no load detection	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 60 mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up, no load detection	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

4,15,22,28,30,31,33,35,36,37 +3VS5
4,33,34,35,36,37,38,39,40 +5VS5
6,13,15,27,28,30,31,32,33 +3VPCU

QCMC

NB5

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB20/30	1A

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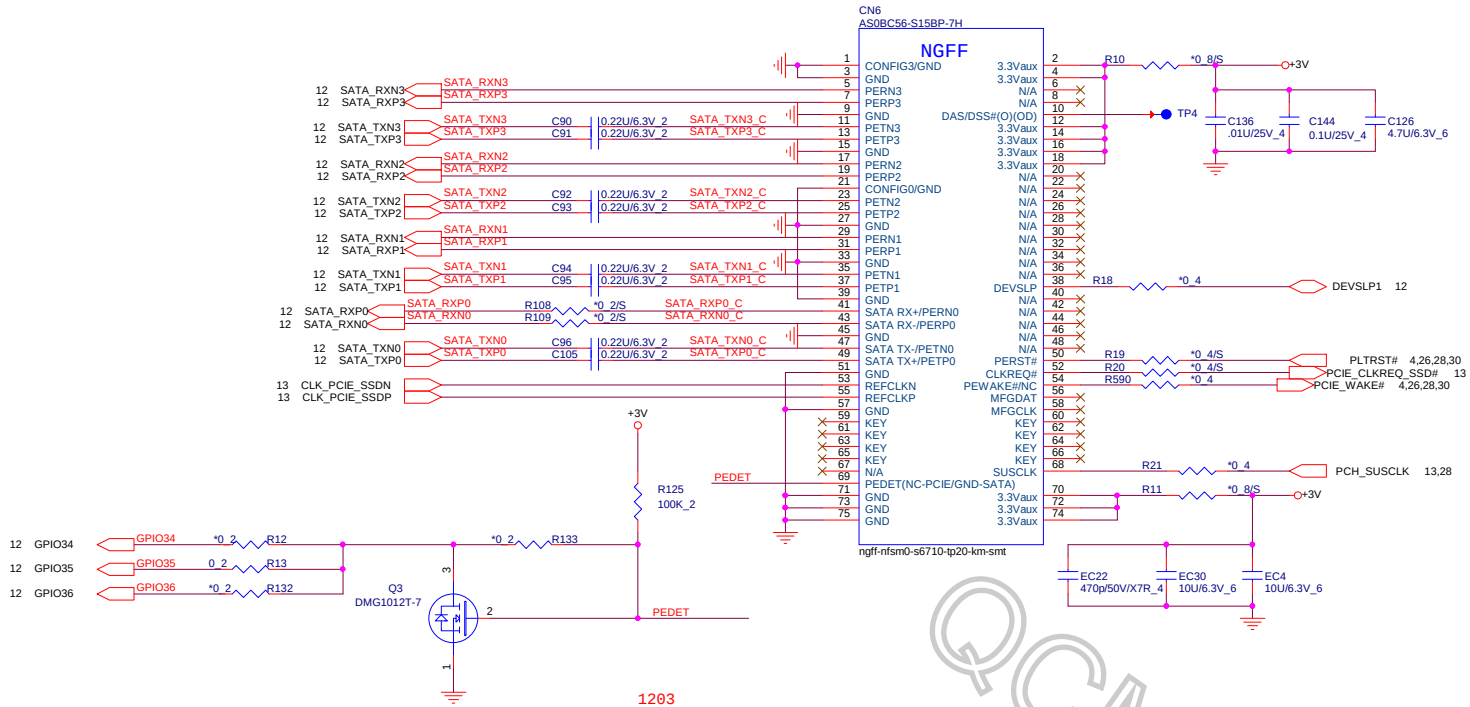
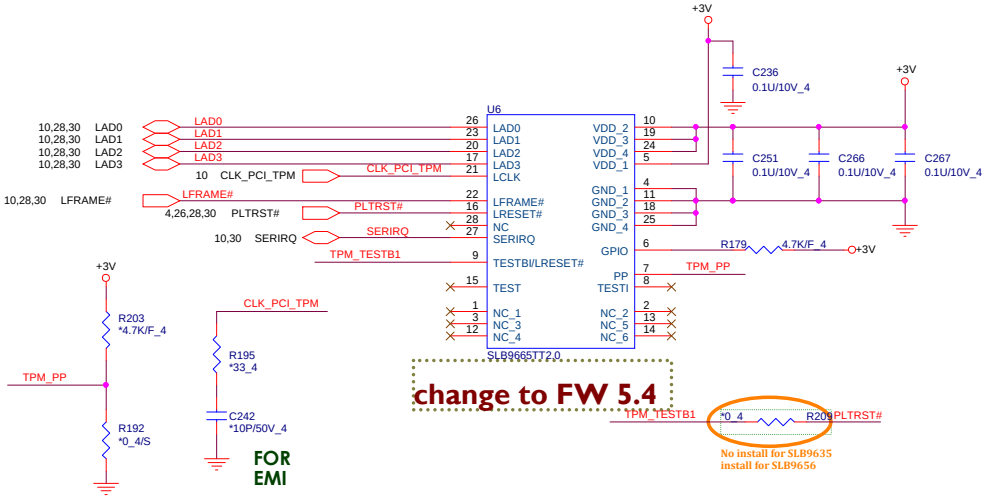


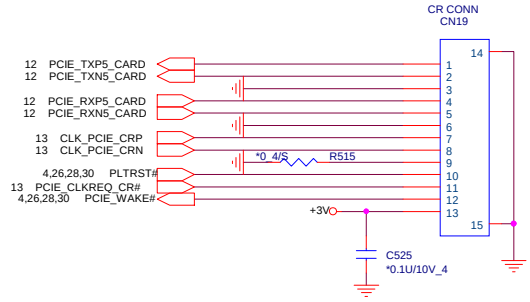
1203
Update footprint from ngff-nfsm0-s6710-tp20-75-km-1 to ngff-nfsm0-s6710-tp20-km-smt

QCMC

TPM (2.0)



Card Reader CON



2,4,10,11,12,13,14,15,20,22,23,27,29,30,31,37,38 +3V
22,23,24,27,37 +5V
6,13,15,27,28,30,31,32,33 +3VPCU

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NGFF HDD/TPM/CR	1A
NB5	Date: Wednesday, January 06, 2016	Sheet 26 of 41

Power Botton

SW2
R104 1K_4
NBSWON1#
NBSWON1# 30
C87 0.1U/10V_4
NTC325-AA1J-A160T
+3V_RTC
LIDEC#
LID_EC# 31
HE1 APX9132H AI-TRG

SI Add for solve leakage

+3VPCU
Q13
LID_EC# 3
Q_LID_EC#
2N7002EPT_SC70

PWR LED

1203
Update footprint from ledl-s110kgct-3p-smt toledltw-110uc5-3p

LED1
DEEP_PWRLED#
3P WHITE LED
R105 200/F_4
+3VPCU
C86 *AVLC 5S
Change from 360ohn to 200ohm for ID

+3VPCU
R103 10K/F_4
DEEP_PWRLED#
Q1 DDTC144EUA-7-F
PWR_LED#
PWR_LED# 30
C85 0.1U/10V_4

Q_LID_EC#
C97 *2.2U/6.3V_6
PV modify

1230
Change net name from SMB_RUN_CLK to SMB_PCH_CLK
Change net name from SMB_RUN_DAT to SMB_PCH_DAT

10 SMB_PCH_CLK
+3V_DEEP_SUS
10 SMB_PCH_DAT
Q22A 2N7002KDW
Dual
Q22B 2N7002KDW
TP_SMB_CLK
TP_SMB_DATA
R348 4.7K_2
R349 4.7K_2
+3VSUS
SUPPORT S3

+3VSUS
+3V_TP
R345 *0_6/S
+3V_TP
R318 4.7K_2 TPDATA
R319 4.7K_2 TPCLK
C336 0.1U/10V_4
CN13
30 TPDATA
30 TPCLK
TP_SMB_CLK
TP_SMB_DATA
TP_CONN_6P
C352 10P/50V_2 TPDATA
C353 10P/50V_2 TPCLK

KEYBOARD Con.

30 MY[0..17]
30 MX[0..7]
MY[0..17]
MX[0..7]
MUTE_LED_CNTL_R1
23 MUTE_LED_CNTL
Q15 2N7002K
R299 10K/F_4
CN11
KB CONN
DFFC32FR041
51586-03201-001-32p-l
MUTE_LED_CNTL_R1 R294 200/F_6 MUTE_LED_CNTL_R
30 CAPSLED#
R293 200/F_6 CAPSLED#_R
30 KB_LED
R292 200/F_6 LED_PWM
+3VS
EC56 *1000P/50V_4

1230
Add EC56 for EMI reserved

1203
Update footprint from 51586-03241-001-32p-l to 51586-03201-001-32p-l

KEYBOARD PULL-UP

MY5 C321 220P/50V_4
MY6 C314 220P/50V_4
MY3 C331 220P/50V_4
MY7 C316 220P/50V_2
MY8 C315 220P/50V_2
MY9 C327 220P/50V_4
MY10 C311 220P/50V_4
MY11 C312 220P/50V_4
MY1 C320 220P/50V_2
MY2 C318 220P/50V_4
MY4 C317 220P/50V_2
MY0 C324 220P/50V_4
MX4 C326 220P/50V_4
MX6 C328 220P/50V_4
MX3 C322 220P/50V_4
MX2 C323 220P/50V_4
MX7 C307 220P/50V_4
MX0 C319 220P/50V_4
MX5 C325 220P/50V_4
MX1 C308 220P/50V_4
MY12 C330 220P/50V
MY13 C329 220P/50V_4
MY14 C313 220P/50V_4
MY15 C310 220P/50V_4

SI

KB backlight

+VIN
R296 1M_4
Q16 AO3404
+5V
30 KB_LED_EN#
Q17 2N7002k
R295 2M_4
C332 0.1U/10V_4
C333 0.1U/10V_4
+5V_LED_KBLIGHT
KB_LIGHT_CONN
CN12

2,4,10,11,12,13,14,15,20,22,23,26,29,30,31,37,38 +3V
22,23,24,37 +5V
6,13,15,28,30,31,32,33 +3VPCU

PROJECT : Y0DD
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	KB/PB/TP	1A

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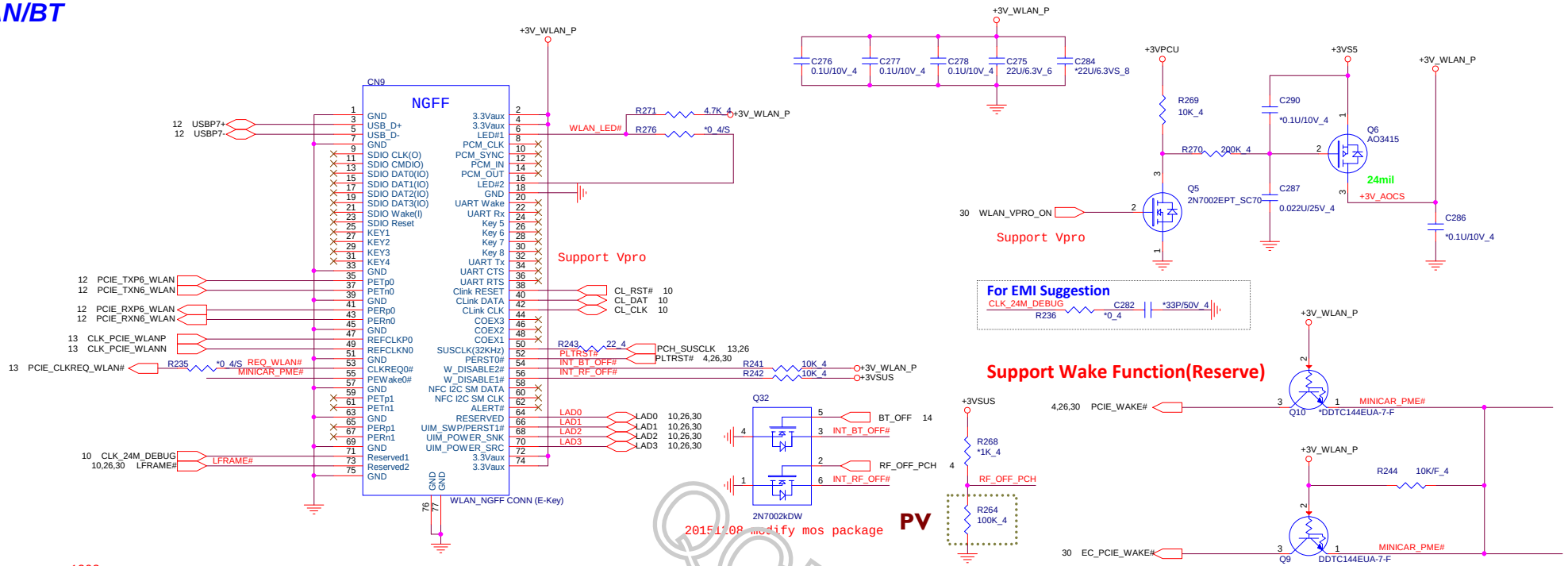
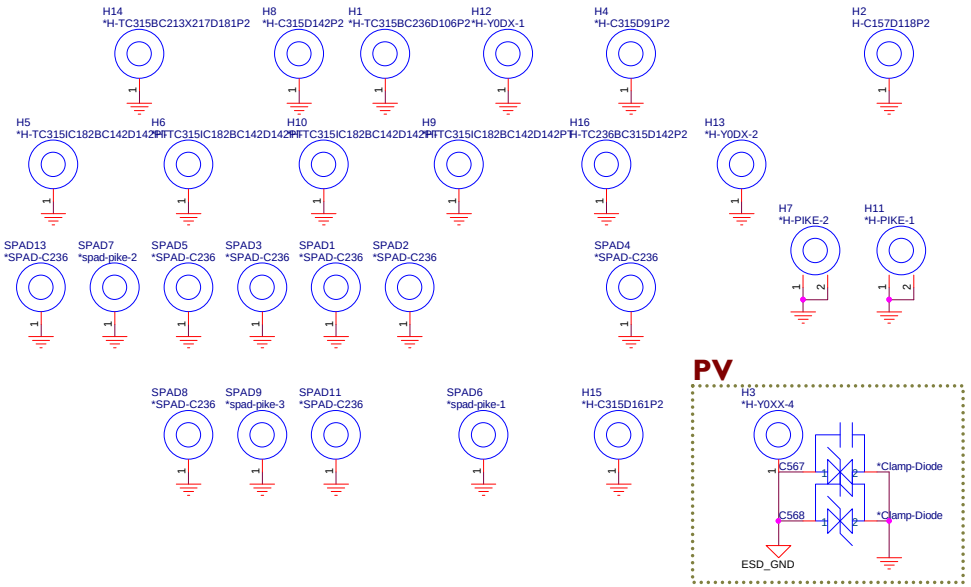
WLAN/BT



Hole

1229
Update H8 footprint from H-C315I142D142P2



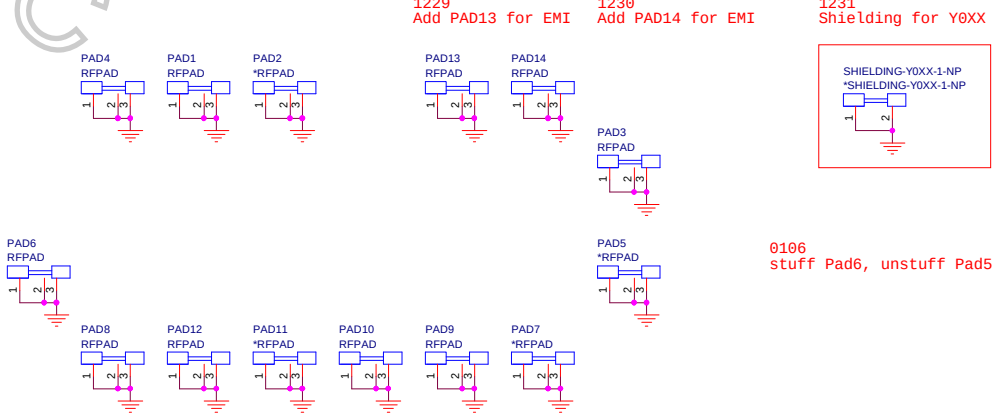
GND GUARD

1229
Add PAD13 for EMI

1230
Add PAD14 for EMI

1231
Shielding for Y0XX

0106
stuff Pad6, unstuff Pad5



QCMC

NB5	PROJECT : Y0DD Quanta Computer Inc.	
Size: Custom	Document Number: WLAN/HOLE	Rev: 1A
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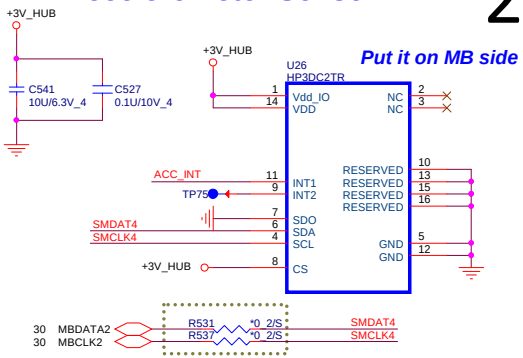
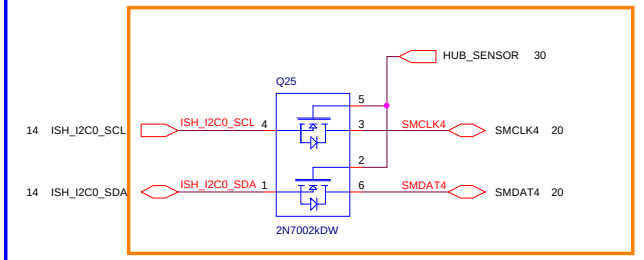
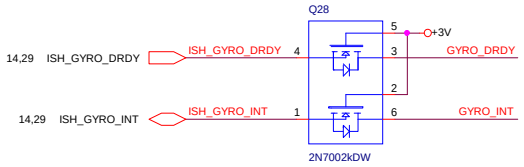
Accelerometer Sensor

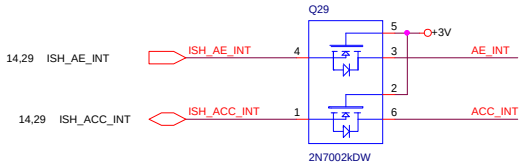


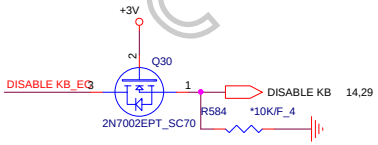


PV add for EC request

1222
Del Q26/ R587/ R588 for OLED reserve

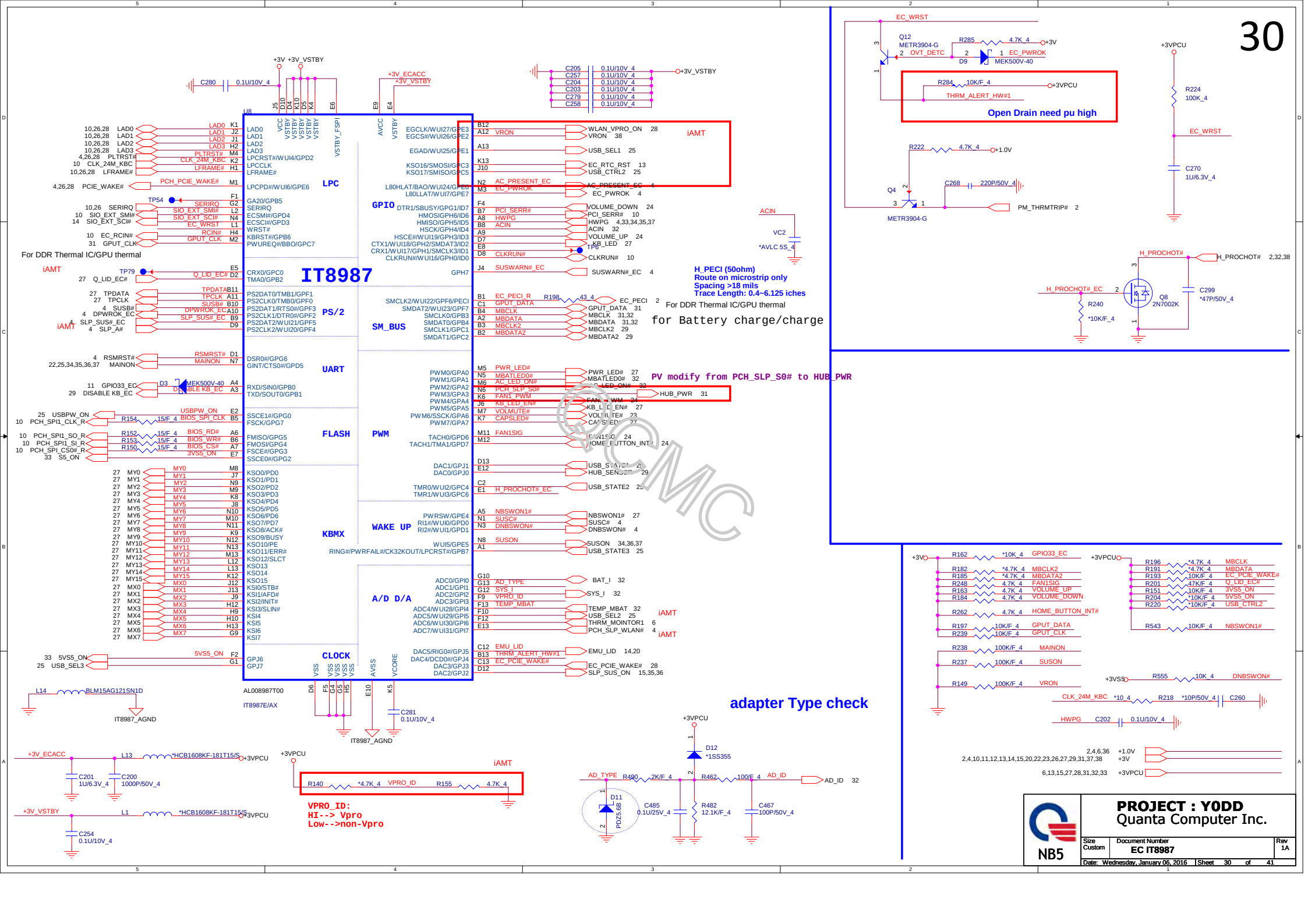


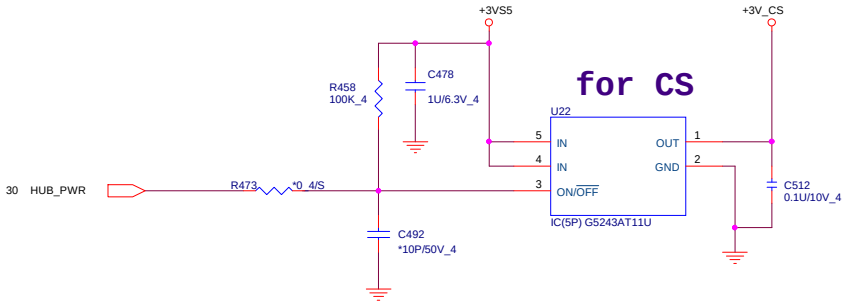


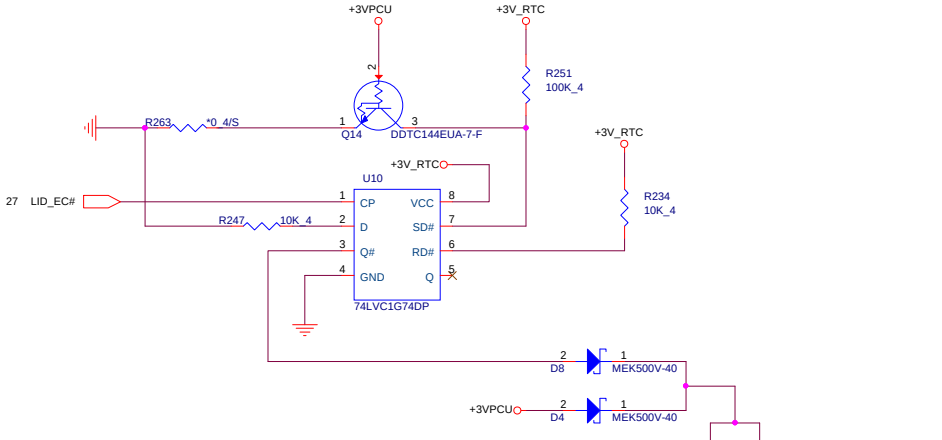


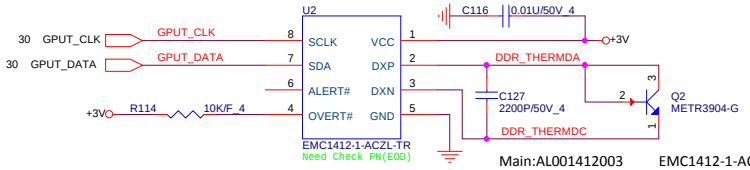
QCMC

NB5	PROJECT : Y0DD Quanta Computer Inc.	
Size: Custom	Document Number: SENSOR HUB	Rev: 1A
Date: Wednesday, January 06, 2016	Sheet 29 of 41	


IT8987
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
iAMT
For DDR Thermal IC/GPU thermal
for Battery charge/charge
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches
PV modify from PCH_SLP_S0# to HUB_PWR
adapter Type check
Open Drain need pu high
VPRO_ID:
HI--> Vpro
Low-->non-Vpro
PROJECT : Y0DD
Quanta Computer Inc.
EC IT8987
NB5
Wednesday, January 06, 2016







Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)
2nd:AL000781039

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.

QCMC

NB5	**PROJECT : Y0DD** Quanta Computer Inc.	
Size: Custom	Document Number: CS	Rev: 1A
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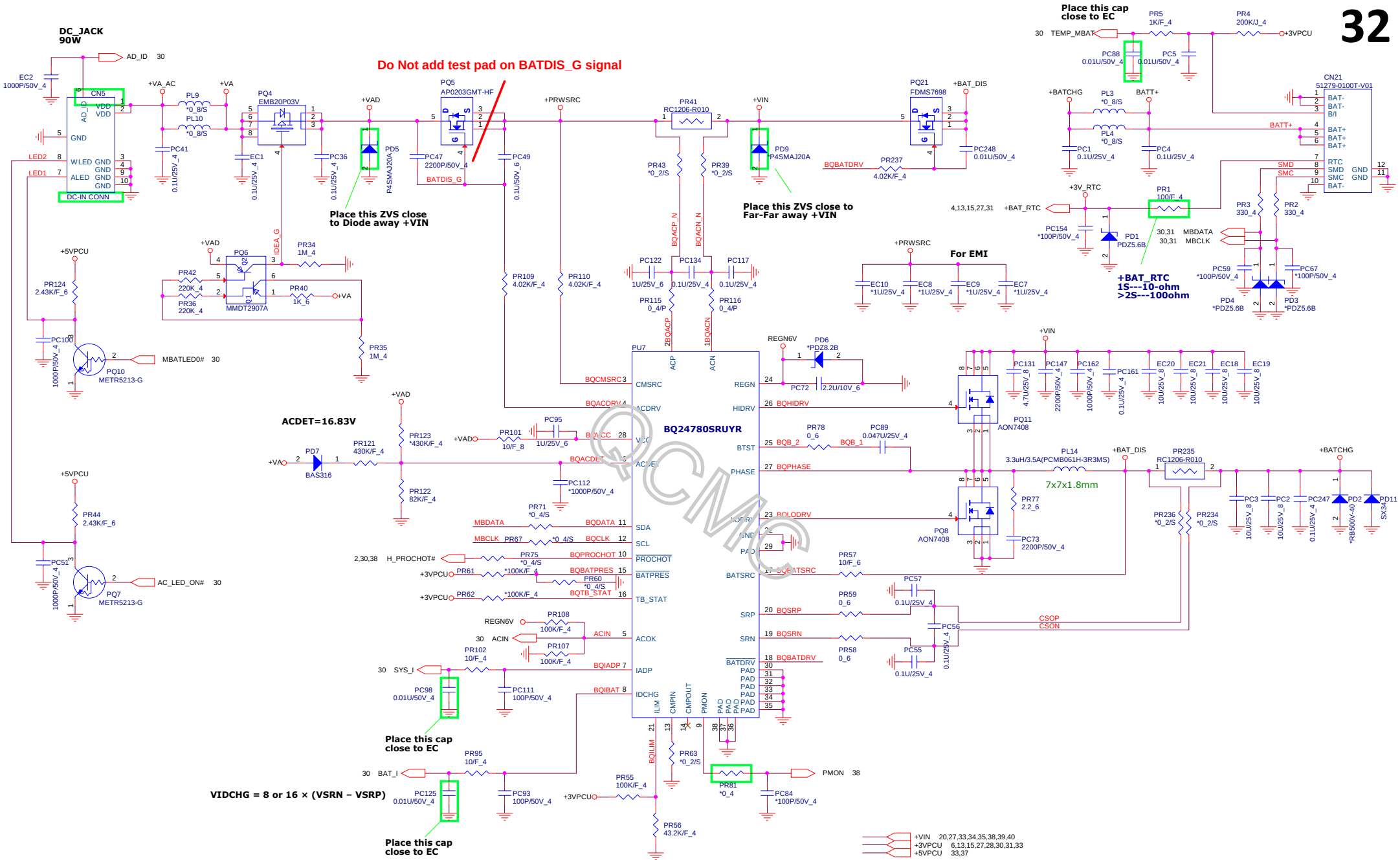
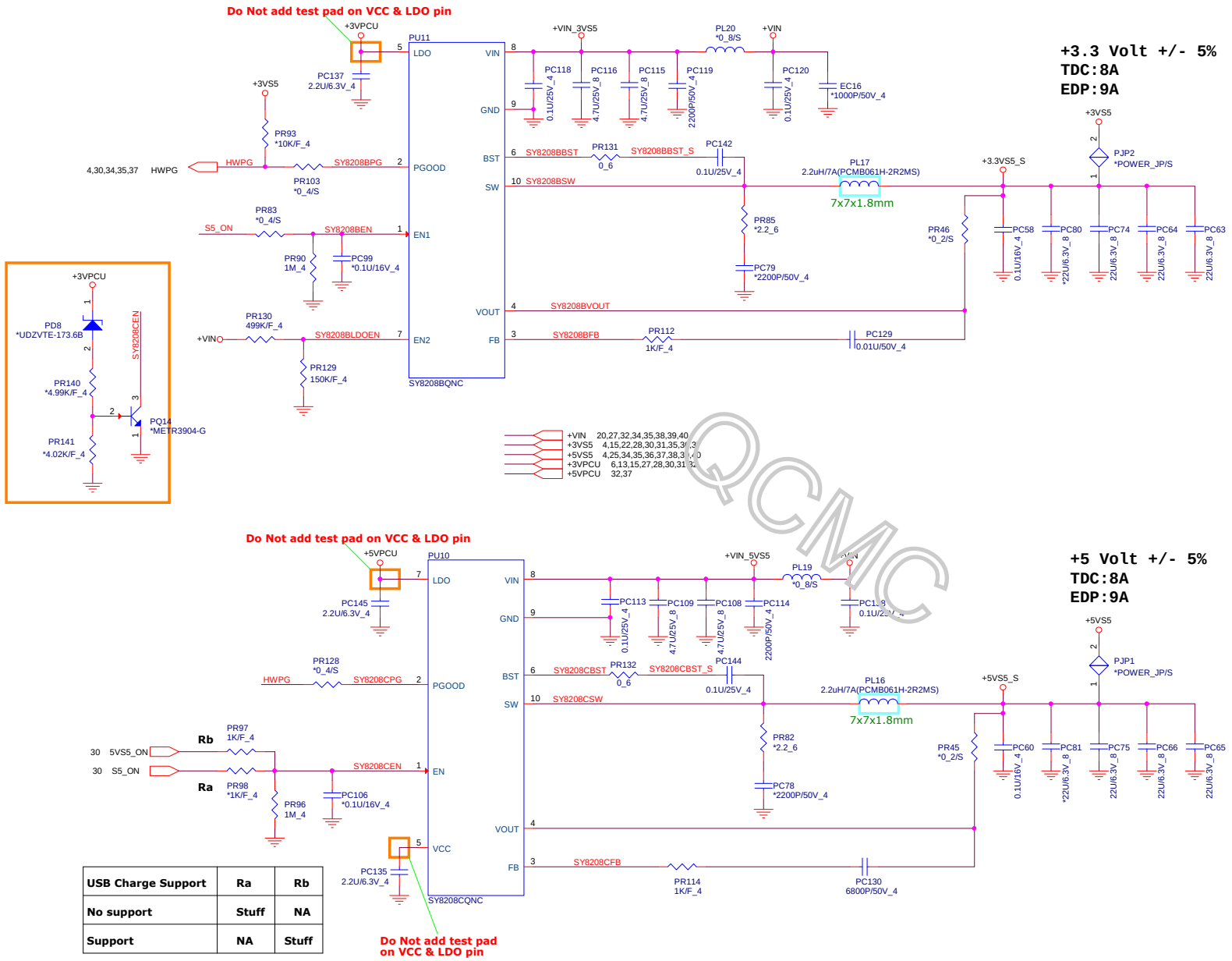


QCMG

NB5	PROJECT : Y0DD Quanta Computer Inc.		
	Size: Custom	Document Number: Charger	Rev: 1A
	Date: Wednesday, January 06, 2016	Sheet 32 of 41	



USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

QCMC

NB5

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5S5	1A

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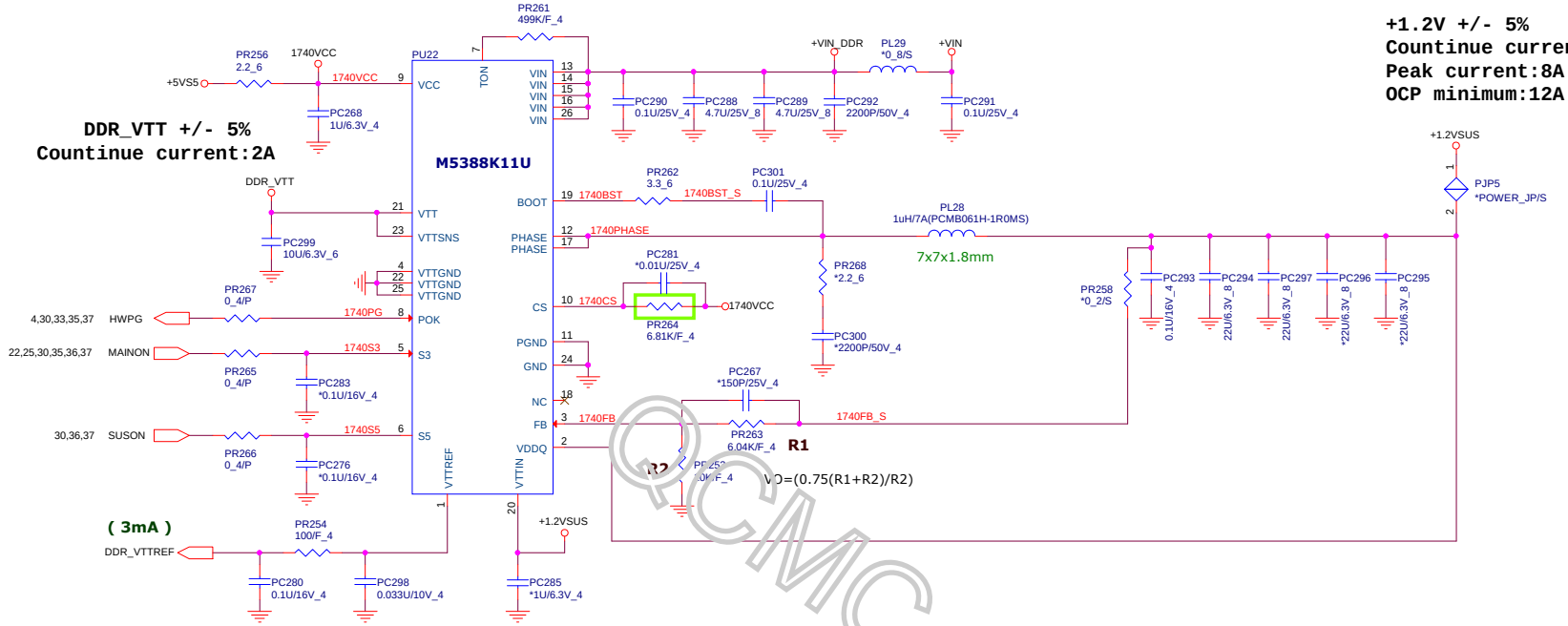
DDR_VTT +/- 5%
Countinue current:2A

+1.2V +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A



QCMC

	S3	S5	+1.2VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

NB5

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR	1A

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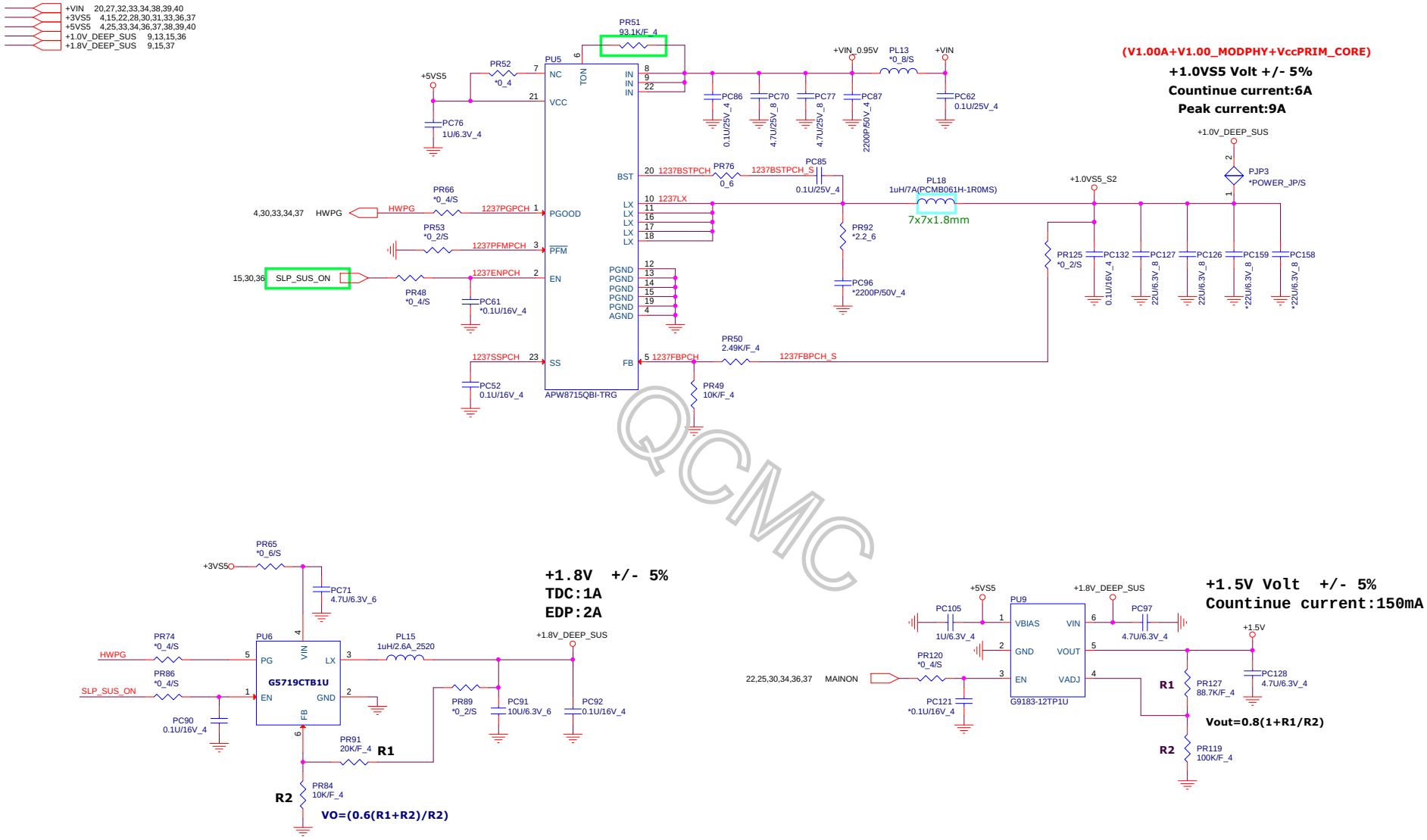

QCMC

NB5	PROJECT : Y0DD Quanta Computer Inc.	
Size: Custom	Document Number: +1.0/+1.5V/+1.8V_DEEP_SUS	Rev: 1A
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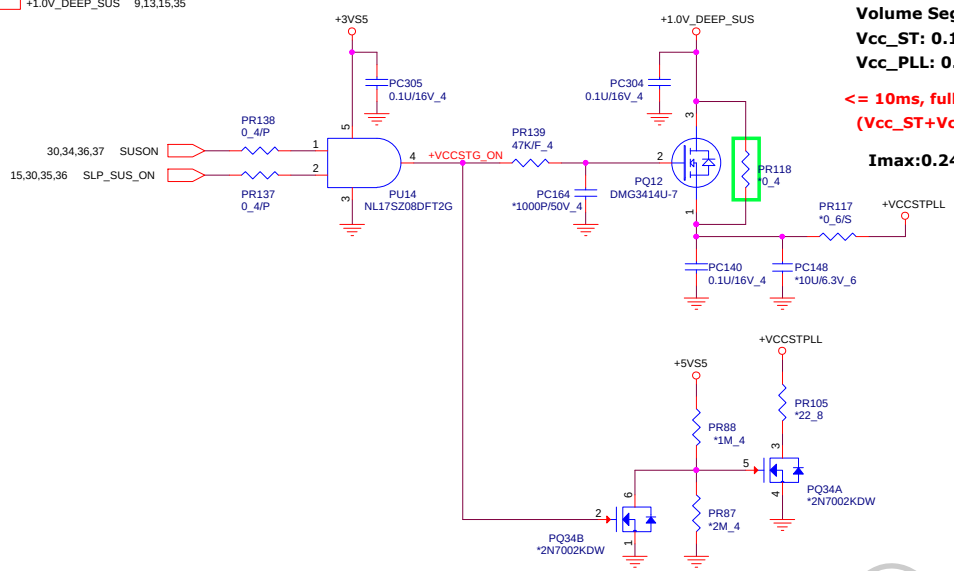
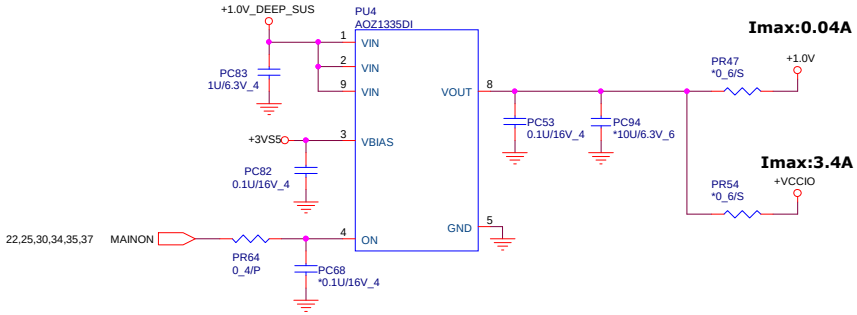
+1.0V 2,4,6,30
+3VS5 4,15,22,28,30,31,33,35,37
+5VS5 4,25,33,34,35,37,38,39,40
+VCCIO 2,6,16
+VCCSTPLL 2,5,6,9,38
+1.0V_DEEP_SUS 9,13,15,35



Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

Imax:0.24A

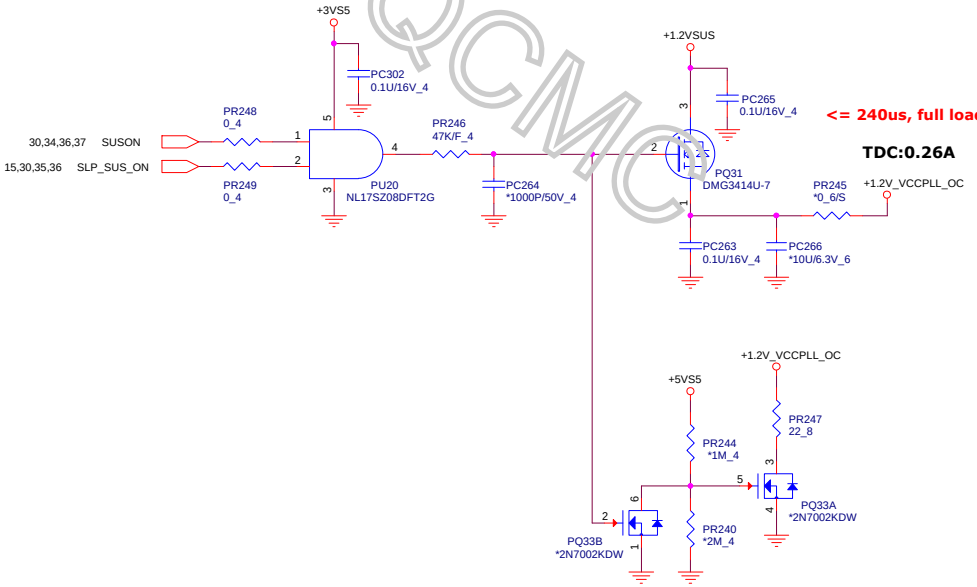


Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

Imax:0.04A

Imax:3.4A



<= 240us, full load ready

TDC:0.26A

QCMC

NB5

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A
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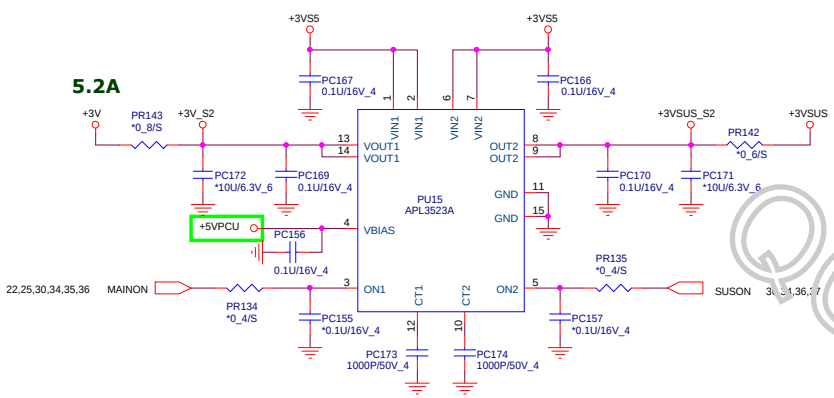
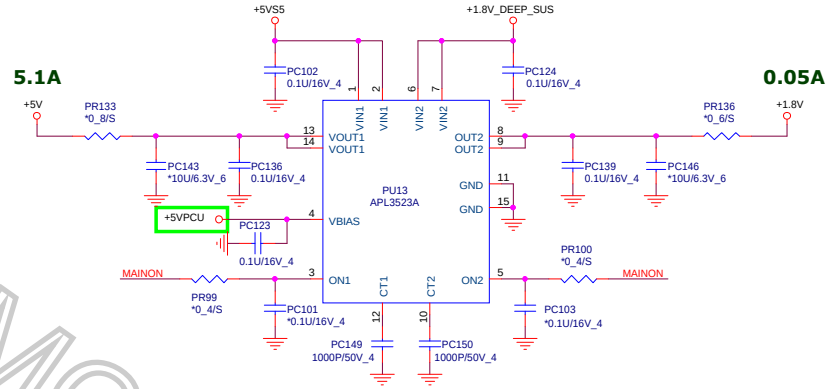
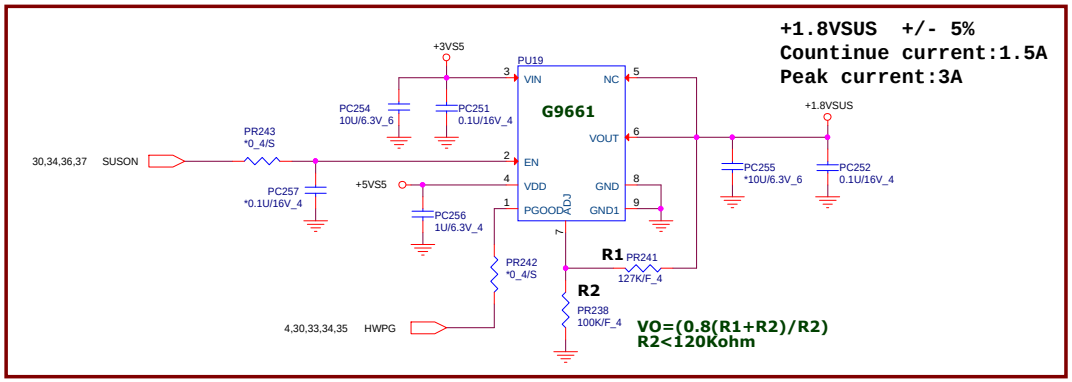
+3V 2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,38
+5V 22,23,24,27,37
+3VS5 4,15,22,28,30,31,33,35,36
+5VS5 4,25,33,34,35,36,38,39,40
+3VSUS 27,28
+1.8V_DEEP_SUS 9,15,35
+1.8V 23
+5V 22,23,24,27,37
+VIN 20,27,32,33,34,35,38,39,40
+1.8VSUS 17,18







QCMC

NB5

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Load switch IC	1A

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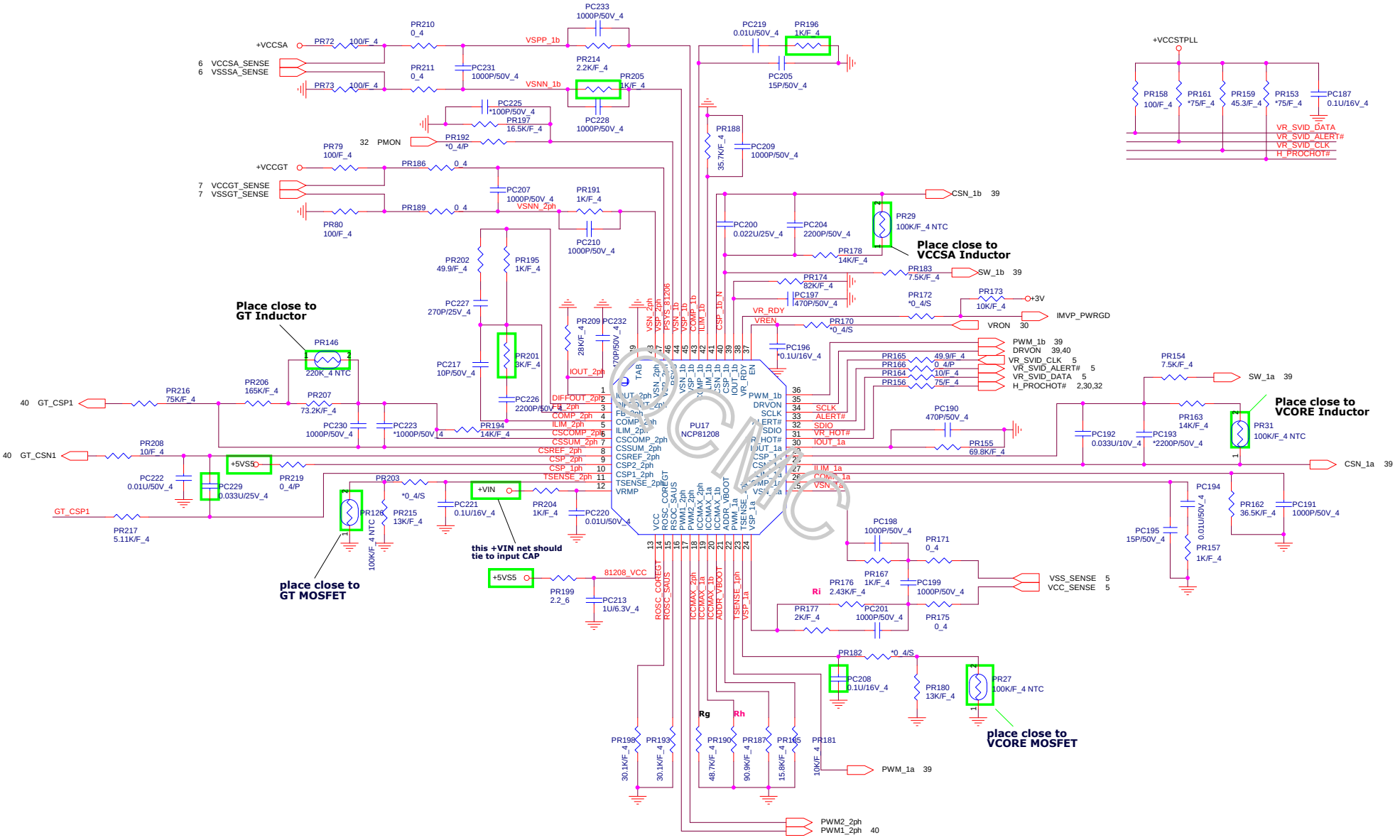
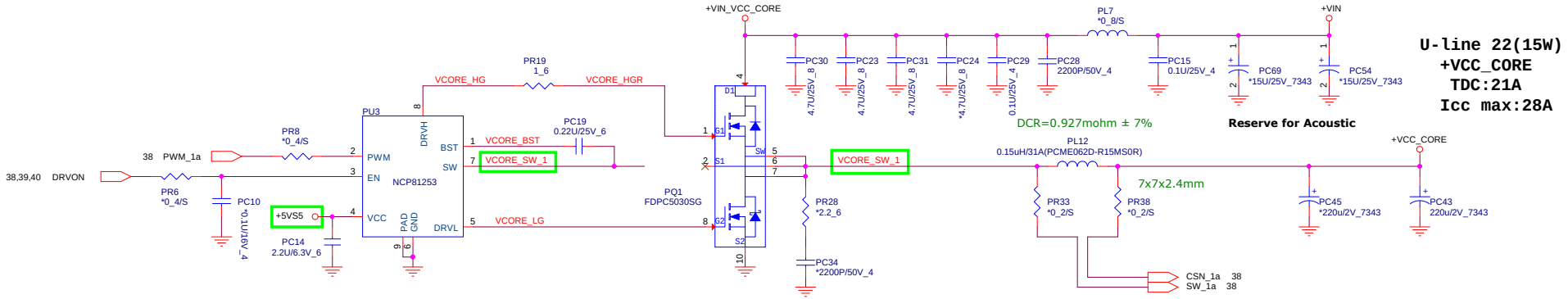
+VCCSA 6,39
+VCCGT 7,40
+5VPCU 32,33,37
+5V 22,23,24,27,37



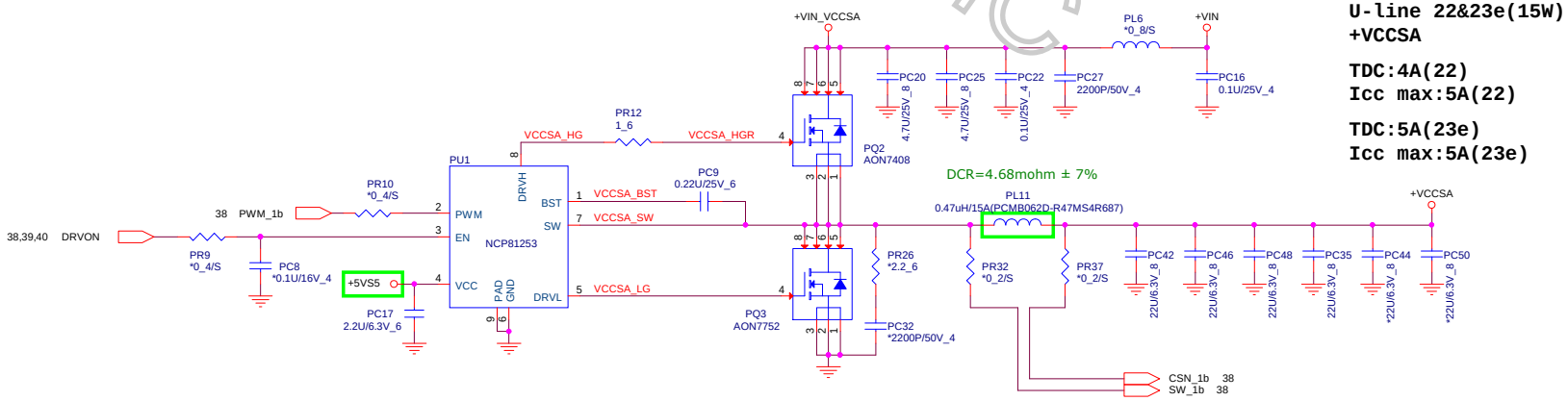
QCT

NB5	PROJECT : Y0DD Quanta Computer Inc.	
Size: Custom	Document Number: CPU VR IC (NCP81208)	Rev: 1A
Date: Wednesday, January 06, 2016	Sheet 38 of 41	

CPU CORE



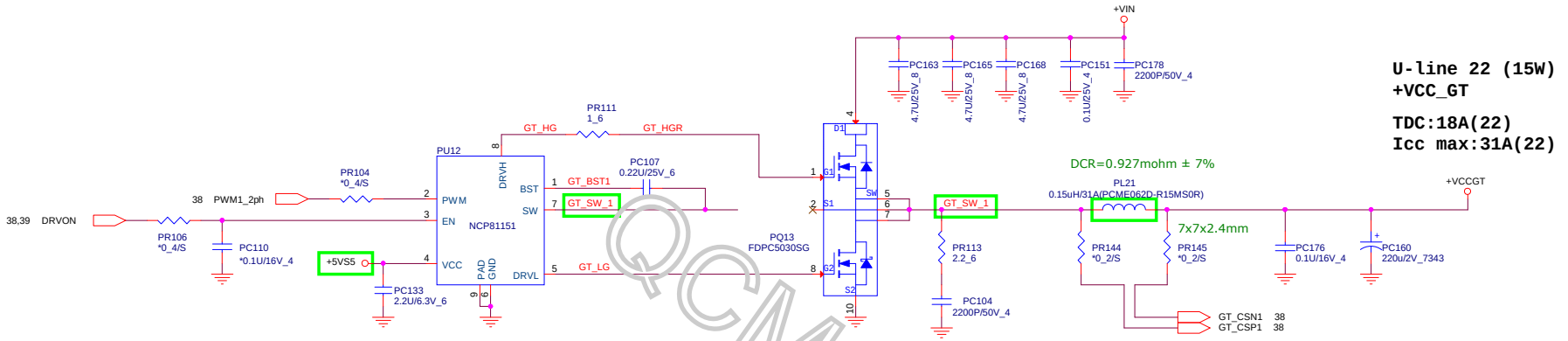
VCCSA



QCMC

NB5	PROJECT : Y0DD Quanta Computer Inc.	
Size: Custom	Document Number: +VCORE/VCCSA (NCP81253)	Rev: 1A
Date: Wednesday, January 06, 2016	Sheet 39 of 41	

+VIN 20,27,32,33,34,35,38,39
+VCCGT 7,38
+VIN_VCC_CORE
+5VPCU 32,33,37
+5V 22,23,24,27,37



U-line 22 (15W)
+VCC_GT

TDC:18A(22)
Icc max:31A(22)

QCMC

NB5	**PROJECT : Y0DD** Quanta Computer Inc.	
Size: Custom	Document Number: +VCCGT (NCP81151)	Rev: 1A
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